

# ATE

## 4230 Advanced Manufacturing Test System

**AEROFLEX**  
A passion for performance.



A compact rack mounted version of the successful 4250 Advanced Manufacturing Test System

- Maximum of 2048 test pins
- Compact 19 inch vertical rack
- Built-in PC system controller
- Microsoft Windows™ operating system
- Software compatible with existing 4200 range
- Automatic Program Generation Software
- Graphical program debug capability
- Analog Auto-Debug
- Vector-less tests
- Capacitor Polarity testing
- CPLD and Flash programming

*The 4230 continues the success of the original 4200 series systems by re-packaging the system hardware into a compact 19-inch chassis. This minimizes the required floor space, a vital requirement for today's high volume mass-market manufacturers. Designed to be used with customized fixturing, the 4230 is flexible enough to be used in both automatic production lines with in-line fixturing or with more conventional bench mounted manual fixtures.*

### System Overview

The 4230 uses the same proven hardware and software as the other 4200 series test systems, the main difference being in the mechanical construction of the system. The compact 19-inch rack cabinet of the 4230 minimizes the floor "foot-print" that is occupied by the system, important in today's environment where space is at a premium.

The 4230 system interface follows the layout of the other 4200 series systems but uses standard 96 way DIN connectors that can be connected via cables to dedicated fixturing. This can either be a simple low-cost table mounted fixture or a more complex automatic production line with a conveyor mounted in-line test fixturing.

### System Architecture

The 4230 is controlled by an integrated industry standard PC running a Microsoft Windows™ operating system. The system's graphical user interface has been designed to provide a familiar environment allowing new users to quickly progress along the learning curve.

The system can be fitted with a range of cards selected from the list below to provide the most appropriate configuration:

- Multiplexed Universal In-Circuit card – This card provides high performance features such as wide ranging drive and monitor voltages (negative voltage capability for ECL testing), learn memory and CRC registers behind each pin, programmable test pin terminators and a host of others. Digital pins are multiplexed by a low ratio of 4:1. In addition, non-multiplexed static guard drivers are also provided, these can be used to control the state of "floating" edge connector inputs.
- General Purpose Input/Output card - This option allows the user to add additional custom hardware to the standard test system to further extend its capabilities. It is also used as a carrier board that can control up to four QMUX boards for implementation of Q-Test II Vector-less tests.

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- Instrument Access card – This option can be used to provide a high quality analog signal path (DC to 80 MHz) to the test fixture for use with external GPIB controlled instruments.
- Analog Functional Card – This includes a 4-channel arbitrary waveform generator and a two channel digital sampler. Used together with the suite of graphical software tools, it allows the system to be used to make a variety of analog functional tests.

### Analog and Digital Testing

The key to low test times is the optimization of analog tests, including contact, shorts and opens. The 4230 offers a combination of high speed and exceptional accuracy through innovative pipeline and parallel processing techniques. A further factor is the utilization of advanced DSP measurements.

High guarding ratios and multi-wire measurement techniques ensure isolation of components and accurate diagnostics during In-Circuit tests. All measurement parameters associated with a test may be adjusted in order to achieve the highest possible accuracy and test stability.

For mixed signal testing, such as ADC, DAC and CODEC devices, the 4230 fully integrates its analog and digital capability. Every test pin is backed by analog and digital resources and their ability to be used in conjunction with each other is a vital element in the testing of these hybrid devices.

Every test pin is provided with both high and low impedance terminators to enable the testing of tri-state buses and open collector devices. Slew-rate controlled pin drivers ensure that vectors delivered to the testpoint have a high integrity and are load tolerant. Where necessary, full back driving protection is provided with programmable time-out and relaxation times.

Clock synchronization and phase locking to 50 MHz is provided to enable the testing of free running devices. Vector rates of 5 MHz with 20 ns edge placement ensure that dynamic devices can maintain keep-alive speed. Testing the most complex VLSI devices requires a range of advanced features such as hardware triggers, pin formatting and variable timing sets, these are all provided as standard. On-the-fly jumps allow for program flow decisions to be made not only within the test program but also in real-time within an individual digital test.

The effectiveness of the 4230 series is further enhanced by the ability to program devices such as FLASH memory and CPLD's from manufacturers such as Xilinx™, Lattice™ and Altera™. This negates the need to invest in further equipment, adding extra value to the In-Circuit stage of the process and reducing the handling of the product.

### Test Program Generation

Test programs are normally generated from the CAD data used to describe the design of the board. The Aeroflex “eM-Test Expert” package (formally known as “FABmaster”) is used to convert from a wide range of CAD formats, producing a .cb format circuit description file. The .cb file is then used to create a test program using the Aeroflex Computer Assisted Program Generation (CAPG) package. CAPG also assists in the design of the test fixture, outputting all the files required to drill and wire of the fixture.

The CAPG user interface is designed to give the test engineer a simple way of creating a test program while ensuring maximum flexibility. CAPG determines the optimum measurement technique for each component and then automatically adds guard points to the test program to remove the effect of the surrounding devices. It then uses an analog circuit simulator to predict the effectiveness of the test, reporting any problems through a series of report files.

This approach ensures that time-to-market for new products is reduced by quick and accurate creation of fixture and program data.

### Test Language

The MTL test language provided with the 4230 provides the user with a high-level structured programming environment with fully integrated edit and debug facilities. The structure of MTL offers the twin benefits of top-level simplicity while also allowing the low level control of all system parameters.

Simple language statements specify ‘packaged’ tests for common measurement types, where the most appropriate stimulus settings and measurement ranges are automatically selected to reflect the circuit configuration. These default settings can be altered by adding modifiers to the standard measurement command through a simple graphical debug panel.

Although a compiled language, MTL offers full interactive edit and debug is achieved through a high-speed incremental compilation process. The overall effect is the speed and power of a compiled language combined with the interactive nature of an interpreted language.

The graphical user interface features a menu system providing control of input/output and peripherals such as barcode readers and printers. Numeric data can be expressed in decimal, hexadecimal, octal and binary formats. Electrical engineering notation (e.g. 10 mV) is also fully supported for application-orientated manipulation of test parameters and results.

### Graphical Debug Tools

A suite of debug tools is used to quickly commission the test program and fixture, again reducing the time-to-market aspects to the test process. In the case of analog measurements, a histogram display is used to dynamically display results with reference to nominal values and tolerances. Digital tests show state and timing information across the whole of the pinface in use during a particular test. Flow trace and test structure diagrams are also provided, fully integrated into the test editors. Each tool within the graphical debug suite gives point and click access to the whole range of parameters applicable to the test.

### Auto-debug

This facility is designed to reduce program development times by using an *automatic debug algorithm* that is independent of the programmer. By altering the measurement parameters and analyzing the results across a number of repeated tests, the auto-debug facility is able to quickly commission a high proportion of the analog In-Circuit tests. The graphical user interface allows user selection of all parameters to ensure the best results. Essentially, the auto-debug facility mimics the actions of a human programmer without the programmer being present.

## Boundary Scan

The 4230 supports the IEEE 1149.1 Boundary Scan standard.

Automatic test generation is provided for boundary scan devices appearing singly or within scan paths. For boards with a scan path consisting of several devices, the 4230 Boundary Scan option can perform interconnect testing for both scan to scan nets and scan nets to physical test pins. These tests are derived from the CAD data describing the board and the BSDL (Boundary Scan Description Language) file pertaining to each device. The process is automatic and fully integrated into the Aeroflex CAPG facility with full manual override available to the programmer if required.

For customers who already have an investment in JTAG Technologies Boundary Scan Test equipment, an optional "JTAG Run-Time Kit" is available for the 4230. The kit allows JTAG Technologies programs to be executed from within the MTL test program. This allows programs and code created during development to be re-used in manufacturing.

## Analog Functional Card

The optional Analog Functional Card (AFC) provides a 4-channel arbitrary waveform generator and a 2 channel 40 MHz digital sampler. The AFC occupies a single slot in the systems test point rack and can be connected to the UUT through the analog bus, direct into the test fixture or via high quality coaxial connections. A suite of visual software tools is provided allowing easy generation and commissioning of test programs using the AFC card. The AFC is perfect for analog functional tests such as testing the frequency response of an amplifier. A swept frequency can be generated by the AFC and applied to the amplifier input, the output signal is then sampled and analyzed using the FFT software tool. The frequency response can then be displayed graphically (for debug) or reported as a simple pass/fail result.

## Third-Party Fixture & Program Compatibility

By using the optional program migration software and an appropriate fixture adapter, the 4230 can be used to transfer production test from a third-party competitive test system. This provides a cost-effective way of replacing older equipment, avoiding high upgrade and maintenance costs. Software migration options are available for Marconi Instruments System 80 / Midata 500 series and various systems from Hewlett Packard, Agilent, GenRad and Philips. For example, the migration method may retain the existing test fixture while CAPG is used to create a new MTL test program. This program will be based on wiring/connectivity data and (where possible) library models that have been extracted from the original program code.

## Fixturing

As mentioned previously, the 4230 system interface is based on 96 way DIN connectors that allow for very flexible fixturing. As we have our own in-house fixturing capability, we are always happy to discuss your specific requirements and can provide quotations for both standard and customized fixturing applications on request.

## Capacitor Polarity

The Aeroflex Capacitor Orientation Defect Analysis (CODA) technique offers a first with a truly reliable and repeatable method of testing for reversed electrolytics. Both single components and parallel sets can be tested and diagnosed down to the failing capacitor. To implement CODA a fixture mounted CMUX card must be fitted with one probe per device. Each CMUX card can provide 8 or 32 channels, ample for most fixtures.

## Vector-less Testing

Aeroflex is unique in offering both inductive and capacitive vectorless techniques, ensuring wide test coverage across a range of components from complex ASICs to connectors. Inductive tests are performed using the Aeroflex patented Q-Test II probe, while the capacitive tests use the low cost CODA capacitor polarity probe. Having these two alternate techniques for vector-less testing allows the test development engineer to use the most appropriate for a given application. These two techniques contribute to the system's ability to generate tests for devices quickly and to accurately diagnose faults to enhance productivity and quality.

# SPECIFICATION

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## GENERAL TEST CAPABILITIES

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*Full In-Circuit Test (Analog, Digital & Mixed Signal)*

*Bus testing & Bus-fail Technique*

*Boundary Scan Test*

*ISP (CPLD) Device Programming*

*Q-Test - Vectorless Tests*

*CODA - Capacitor Polarity Tests*

*Analog Functional Card "AFC" (Optional)*

## SYSTEM CONTROLLER

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*Pentium Class Processor*

*256 MBytes Memory*

*Windows Operating System*

*TFT Flat Screen monitor*

*IEEE-488 interface (Optional)*

*CAN Bus interface (Optional)*

*Bar Code Reader (Optional)*

## TESTPOINT COUNT

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*128 - 2048 Universal Test Points*

*128 Test Points per card. Digital Multiplexing Ratio of 4:1*

## ANALOG TEST FACILITIES

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### Contact Test

*< 100 k $\Omega$*

### Shorts Test

*1 to 100  $\Omega$*

**Link Test**1 to 100  $\Omega$ **Resistance DC**0  $\Omega$  to 10 M $\Omega$ **Resistance AC**0  $\Omega$  to 1 M $\Omega$ **Capacitance AC**

0 pF to 100 mF

**Capacitance DC**1  $\mu$ F to 100 mF**Inductance**

0 H to 100 H

**Diode**

ON &amp; OFF

**Zener**

Voltage

**FET**

ON, OFF &amp; RDS

**LED**

ON &amp; OFF

**Transformer**

Ratio 0.001 to 100

**Opto-Isolator**

ON

**Transistor**

ON, OFF &amp; HFE

**GENERAL PURPOSE ANALOG FACILITIES**

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**DC Stimulus (2 off)**

1 mV to 25 V

0 A to 100 mA

**AC Voltage Stimulus**

0.1 V to 20 V pk-pk

**Frequency**

0.1 Hz to 20 kHz

**Waveforms**

sine, square, triangle, ramp up, ramp down

**DC voltage Measurement**0 V to  $\pm$ 50 V**DC current Measurement**0 A to  $\pm$ 100 mA**AC voltage Measurement**

0 V to 50 V

**Frequency Measurement**

0.02 Hz to 5 MHz

**Period Measurement**10  $\mu$ s to 65 s**Programmable Resistor**0  $\Omega$ , 1  $\Omega$  to 10 M $\Omega$  in decade-steps**1149.1 BOUNDARY-SCAN FACILITIES (OPTION)**

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Any standard test pin may be used to perform Boundary-Scan tests. A configurable memory is accessible to all test pins providing the serial data needs for Boundary-Scan testing and permitting support for multiple scan paths.

**Supported Tests**

Integrity (Infrastructure) tests

Interconnection tests:

Stuck &amp; Open pins

Shorts (Scan to scan)

Shorts (Scan to test pin)

**DIGITAL TESTING**

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Digital testing is full parallel drive, parallel sense.

**Pattern Rate**

Maximum of 5 MHz (200 ns)

**Internal Clock Frequency**

50 MHz

**Clock Divider**

1 to 256

**Timing Sets**

4

**Formats Per Timing Set**

6 (NRZ, RZ, DNRZ, R1, RI &amp; RC)

**Hardware Event Triggers**

4

**External Clock Input**

2 MHz - 50 MHz

Phase Lock to a Maximum Frequency of 50 MHz

Pattern Generators (Shift, Rotate, Increment) Accessible To All Pins

**Flow Control Instructions**

NOP, IF(NOT), CALL, RETURN, JUMP, DELAY, LOOP, EXITLOOP, ENLOOP, REPEAT, UNTIL, STOP, PAUSE

**Max Input Voltage**

-50 V to +50 V (logic relay open)

**Control RAM depth**

8 K

**Flow trace RAM**

64 K

**MULTIPLEXED TEST POINT CARD (FA03)**

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**Signature Analysis (CRC)**

Per Pin

**Logic Families**

1 Per Board

**Drive High Voltage Range**

-1.0 V to +14 V

**Drive Low Voltage Range**

-6.0 V to +1.0 V

**Sense Levels**

-8.0 V to +15 V

**Drive High/Low Current**

500 mA (forcing) 50 mA (non-forcing)

**Slew Rate**

50 V/ $\mu$ s (slow) 150 V/ $\mu$ s (fast)

**Backdrive Timeout**

10  $\mu$ s to 650 ms

**Relaxation Timer**

1 ms to 10 s

**Test pin RAM Depth**

8 K

**Pin Face Skew**

20 ns Maximum

**Digital Guarding**

2 Static Guards per TP Board: One Drive High, One Drive Low

**DEBUG FACILITIES**

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Manual Probe for In-Circuit & Fixture Debug

Pin Search Function

**UUT POWER SUPPLIES**

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Maximum of 6 supplies

2 Types Available:

0.60 V to 6.0 V, 23 A Voltage and Current Programmable

3.0 V to 30.0 V, 6.5 A Voltage and Current Programmable

**SYSTEM SOFTWARE MTL TEST LANGUAGE**

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High Level, Function Based, Structured Programming Language

Interactive Edit and Debug Facilities

System Self Check Software

System Self Calibration Software

Computer Assisted Program Generator "CAPG" (Optional)

32 bit Windows Application

Generic Device Library

CAD (.cb file) or Manual Input

Safe Check Digital Back-Driving Analysis Software

Bus Test Generation

ISP / CPLD Device Programming (Xilinx, Lattice, etc)

Boundary-Scan Test Generation (Optional)

Multi-Board & Panel Testing (Optional)

**OPTIONAL SOFTWARE**

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**i-Base5 Information Management System (Optional)****Software Migration Tools (Optional)**

Options for:

Agilent / HP3070 series

GenRad 2270 / 2280 series

IFR / Marconi System 80 series

Philips ICCT2000

eM-Test Expert (formally FabMaster)

**OPERATING CONDITIONS**

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**Mains Supply**

180 to 264 volts, 47 Hz to 63 Hz, AC Single Phase 13A

110 V Option also available

**Power Consumption**

2 kVA

**Operating Temp Range**

+10°C to +35°C

**Humidity Range**

25% RH to 75% RH

**DIMENSIONS**

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**Height**

1700 mm (max)

**Depth**

1000 mm (max)

**Width**

700 mm (max)

**Weight**

180 kg (Approximate)

**Fixturing**

Flexible to meet requirements

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Our passion for performance is defined by three attributes represented by these three icons: solution-minded, performance-driven and customer-focused.