

Application Note

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FASTBIT FB100A

MEASURING BER OF DEVICES WITH UNIQUE SERIAL AND PARALLEL INTERFACES



Flexible interfacing enables sub-system design
verification and test.

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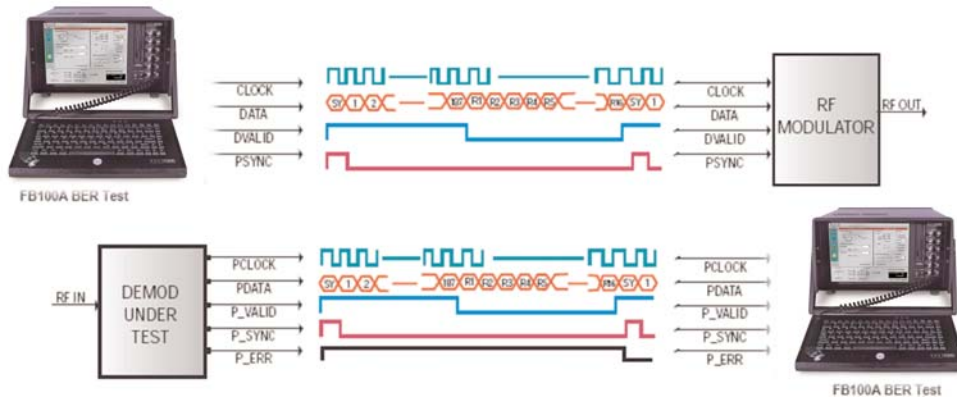


Figure 1. Typical setup for direct interfacing to DEMOD under test and modulator

TECHNICAL HIGHLIGHTS

- R&D and DVT engineers can interface directly to demo boards and modulators
- New standards are supported through user programmable I/O
- Most commercial modulator data interfaces supported directly
- DOCSIS, DVB, DAVIC standards patterns pre-programmed

RELATED APPLICATION NOTES

- BER ANALYSIS USING FRAMED DATA
- AUTOMATED BER PLOTS USING FB100A BER TEST SYSTEM AND INTEGRATED NOISE AND IMPAIRMENT MODULE
- BER TEST TIME OPTIMIZATION
- MEASURING 'IN-CIRCUIT' BER ON LIVE DATA

INTERFACING BERTS TO THE DUT AND MODULATOR

Interfacing to today's demodulator chipsets and the necessary test modulators presents a significant challenge. Traditional BERTs require add-on interface circuitry that distracts R&D and DVT engineering from product development. Engineering needs to address several issues: Is the interface serial or parallel? What handshaking signals are needed? Are framing bytes needed? What are the logic levels and signal timing? For example, DVB document A010 describes 188 byte and 204 byte transmission modes. In the 204 byte mode, DVALID is disabled during Reed Solomon correction bytes. This document also describes the Synchronous Parallel Interface (SPI) that uses LVDS logic levels, and maps data, clock and I/O to a DB25 connector. Chipset manufacturers have augmented this I/O with signal additions, such as P_ERR (DFAIL), to indicate frames that weren't corrected by the embedded error correction. Serial derivatives of this approach are also in common use in the industry.

THE FB100A OFFERS FLEXIBLE PARALLEL AND SERIAL INTERFACES

With its MPEG pods, the FB100A fully supports the DVB Synchronous Parallel Interface or the DVB Asynchronous Serial Interface (ASI) using interface "Pods" at its rear panel Data Generator output and Error Analyzer input. The serial version of the synchronous interface is available at the test set's front panel. Also, a variety of Pods and front panel selections are available providing standard logic levels and interfaces. PECL, ECL, TTL, RS-422, ASI, OC3, and LVDS are available, allowing the engineer to connect to most commercially available modulators and DUTs. Pods with high impedance I/O are available, allowing direct connection to IC outputs and test headers. The FB100A provides user defined control of the I/O through an on-board pattern editor, allowing demodulator engineers to support a wide range of devices and standards.

CREATING PATTERNS AND CONTROL SIGNALS

The FB100A generates 3 types of patterns: straight pseudorandom bit sequences (PRBS), programmed byte patterns (WORD) and patterns with a mix of PRBS and WORD bytes (MIX). The MIX control is done via a separate pattern, the MIX pattern. The MSB of the MIX pattern is used to control the multiplexing of PRBS and WORD patterns. For detailed programming information, please review the "FB100A Operations Manual".

MIX Pattern Features

- It is not used when generating or analyzing a straight WORD pattern or PRBS pattern.
- The PRBS pattern generator stops during selected WORD bytes in a MIX pattern.
- The WORD pattern does not stop during selected PRBS bits therefore it must be the same length as the MIX pattern, and filled with zeroes during PRBS bytes (0's in the MIX pattern).

In Serial mode,

Data bit 2 (bit d2) of the MIX pattern is routed to the SYNC2 output to be used as a "valid byte" indicator (DVALID).

In Parallel mode,

Data bits d2 and d0 of the MIX pattern are special bits that are directed to the output to be used as auxiliary signals (PSYNC, DVALID), or as additional pattern bits (d9, d10). D2 and D0 are connected to the PSYNC and DVALID pins, respectively, of the Synchronous Parallel Interface for CATV/SMATV Headends.

SAMPLE WAVEFORM - MPEG TRANSPORT SERIAL AND PARALLEL OUTPUT

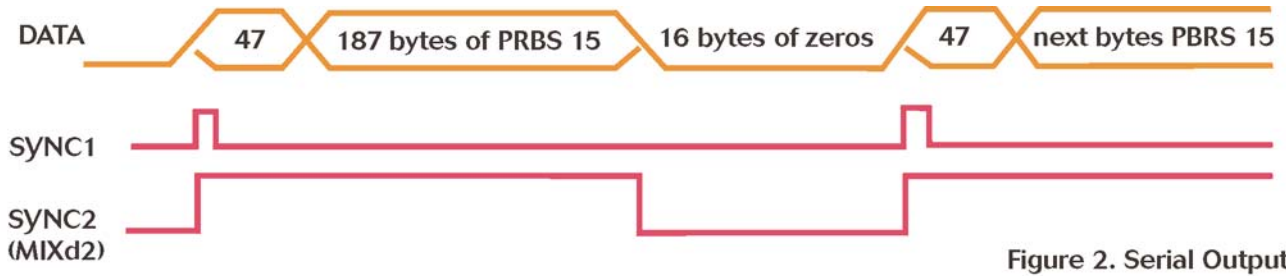


Figure 2. Serial Output

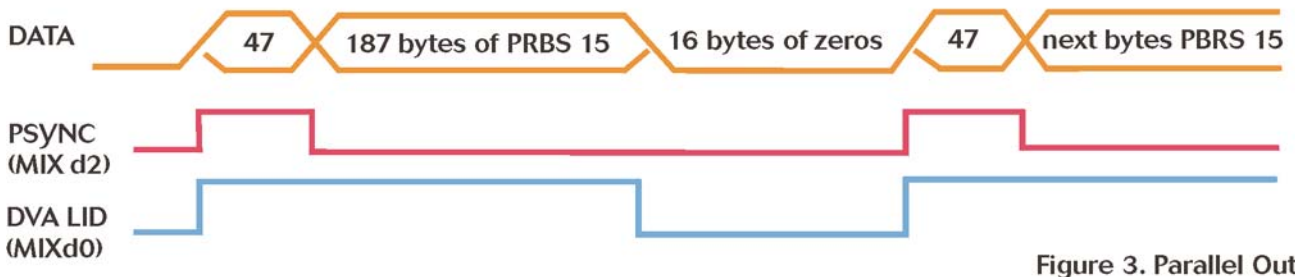


Figure 3. Parallel Output

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