

Application Note

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FASTBIT FB100A

BER TEST TIME OPTIMIZATION



Automated BER vs. Eb/No testing gives high accuracy results with dramatic reduction in test times.

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TECHNICAL HIGHLIGHTS

- Software includes theoretical curves for performance comparisons
- User can specify accuracy and confidence factors for each Eb/No point to optimize speed of test
- Software pre-calculates test time based on user defined parameters
- Test setup is completely automated by resident software, and internal noise and interference impairment generator

RELATED APPLICATION NOTES

- BER ANALYSIS USING FRAMED DATA
- AUTOMATED BER PLOTS USING FB100A BER TEST SYSTEM AND INTEGRATED NOISE AND IMPAIRMENT MODULE
- CABLE MODEM PHY PERFORMANCE EVALUATION
- MEASURING BER OF DEVICES WITH UNIQUE SERIAL AND PARALLEL INTERFACES

FB100A BER CALCULATOR LOWERS TEST TIME

Performance of digital RF demodulators is typically characterized by measuring BER over a range of carrier to noise ratios. Results are usually compared to theoretical values, or other competitor's published results.

Prior to performing actual BER measurements in the lab, decisions can be made regarding accuracy, confidence level and best-case BER in order to limit test times.

By understanding the relationships between accuracy, confidence level and test times, tradeoffs can be made to best use the available testing time.

When performing BER measurements, bit errors might occur or might not.

When bit errors occur, the specified accuracy and confidence factor determine the number of bit errors required to be measured. Based on assumptions of error distribution, bit rate and best case BER, a time estimate is calculated.

When the measurement is error free, the total number of measured bits required is governed by the confidence level of a best-case BER. Based on the bit rate, another test time is also calculated. The larger test time of both scenarios is displayed.

COMPARISON AGAINST THEORETICAL CURVES

Demodulator engineers want to test their product against theoretical curves for various modulation formats and error correction schemes, e.g. QPSK, 64QAM, 256QAM with Viterbi, Trellis and Reed-Solomon error correction.

Theoretical curves can be used to define the best-case BER scenarios used in pre-calculating BER test times. One may find, however, that the device under test's performance deviates significantly from theory, especially at high Eb/No values

In these cases, lower test time estimates can be achieved by picking a best-case BER worse than theory.

CREATING PATTERNS AND CONTROL SIGNALS

The FB100A generates 3 types of patterns: straight pseudorandom bit sequences (PRBS), programmed byte patterns (WORD), and patterns with a mix of PRBS and WORD bytes (MIX). The MIX control is done via a separate pattern, the MIX pattern. The MSB of the MIX pattern is used to control the multiplexing of PRBS and WORD patterns. For detailed programming information, please review the "FB100A Operations Manual".

MIX Pattern Features

- It is not used when generating or analyzing a straight WORD pattern or PRBS pattern.
- The PRBS pattern generator stops during selected WORD bytes in a MIX pattern.
- The WORD pattern does not stop during selected PRBS bits therefore it must be the same length as the MIX pattern, and filled with zeroes during PRBS bytes (0's in the MIX pattern).

In Serial mode

Data bit 2 (bit d2) of the MIX pattern is routed to the SYNC2 output to be used as a "valid byte" indicator (DVALID).

In Parallel mode

Data bits d2 and d0 of the MIX pattern are special bits that are directed to the output to be used as auxiliary signals (PSYNC, DVALID), or as additional pattern bits (d9, d10). D2 and D0 are connected to the PSYNC and DVALID pins, respectively, of the Synchronous Parallel Interface for CATV/SMATV Headends.

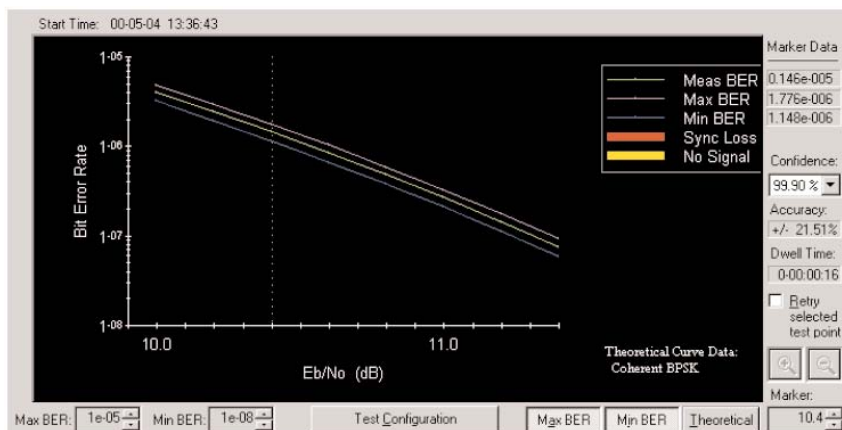


Figure 1. Typical setup for automated BER vs. EbNo testing

SAMPLE WAVEFORM -

MPEG TRANSPORT SERIAL AND PARALLEL OUTPUT

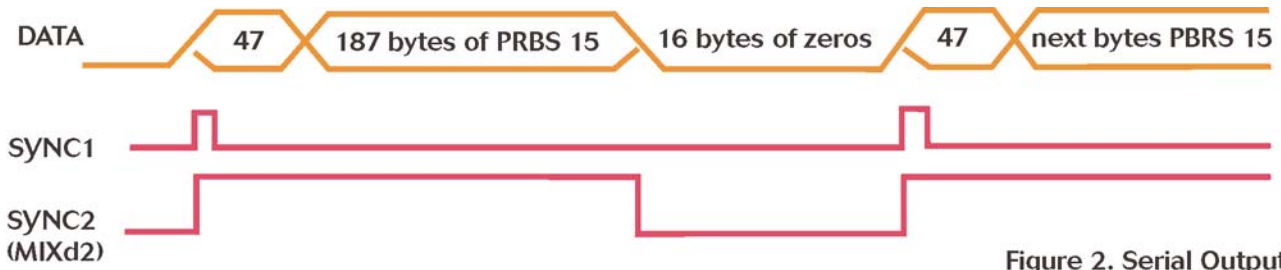


Figure 2. Serial Output

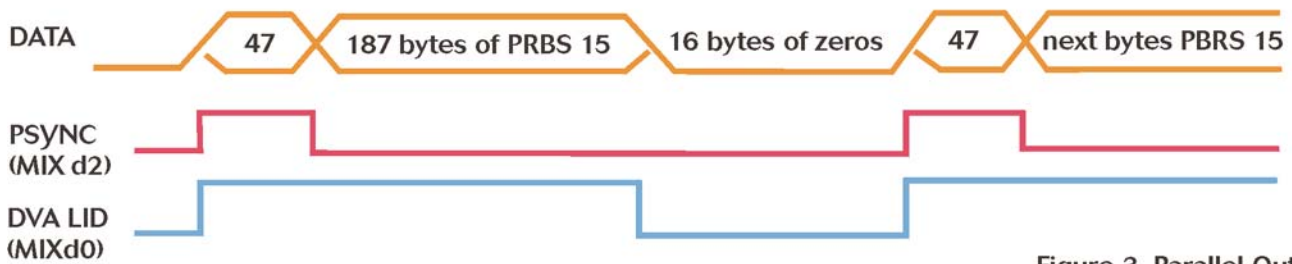


Figure 3. Parallel Output

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Part No. 46891/935, Issue 1, 01/05