

UTMC PRODUCT ADVISORY

BCRT Family Built In Test Anomaly

UTMC has identified the following anomalous behavior in all production revisions of the UT1553 BCRT/BCRTM/BCRTMP(i.e., UP04, UP17, and UP11):

Background:

The UT1553 BCRT Family implements a built-in test (BIT) function that results in a fault coverage of approximately 45 percent. The BIT is invoked by either the host microprocessor or a 1553 message. The host microprocessor initiates the BIT by writing to the BIT Start Register (Register #11). The host microprocessor reads the BIT Word Register (Register #4) to determine the outcome (i.e., pass or fail) of the BIT. In the remote terminal (RT) mode of operation, the 1553 bus controller initiates a RT self-test by issuing an Initiate Self-Test Mode Code command to the RT. The bus controller observes the BIT results by issuing a Transmit BIT Word Mode Code command.

UTMC literature recommends the following microprocessor I/O sequence to initiate a BIT:

- Write to the Program Reset Register (Register #12)
- Wait 1 μ s for reset to take place
- Write to the BIT Start Register (Register #11)
- Wait 100 μ s for BIT to complete
- Read the BIT Word Register (Register #4)

The write to Register #12 stops device operation (i.e., BC, RT, or monitor) and prepares the device for BIT. The write to Register #11 initiates the BIT, reading Register #4 determines the BIT outcome.

A recent evaluation determined the UT1553 BCRT family of products exhibits anomalous behavior during host initiated BIT sequences in the presence of MIL-STD-1553 bus traffic. When using the above I/O sequence, in the presence of bus traffic, the BCRT product intermittently reports BIT failures in Register #4 (either channel A or B). If no MIL-STD-1553 bus traffic is present the above I/O sequence does not result in any BIT failures.

Work-Around:

To prevent the generation of BIT failures in the presence of bus traffic, modify the microprocessor I/O sequence as follows:

- Master Reset
- Write to the BIT Start Register (Register #11)
- Wait 100 μ s for BIT to complete
- Read the BIT Word Register (Register #4)