

# UTMC PRODUCT ERRATA

## BCRT Family Revised AC Electrical Characteristics

The following tables contain revised timing for the UT1553 BCRT Family of devices. Numbers contained in brackets indicate the previous limit. Refer to the UTMC 1553 Product Handbook for the timing diagrams associated with these parameters.

**Table 1:**

Symbol	Parameter	Minimum	Maximum	Units
$t_{OOZL1}$	$\overline{DMAR} \downarrow$ to BURST $\uparrow$	-10 (0)	+10	ns
$t_{SHL1}$	ADDRESS valid to $\overline{RRD} \downarrow$ (ADDRESS setup)	THMC2 - 10 (THMC2 - 20)	THMC2 + 5 (THMCS)	ns
$t_{PW1}$	$\overline{RRD} \downarrow$ to $\overline{RRD} \uparrow$	MCLK - 10 (MCLK - 5)	MCLK + 5	ns
$t_{HLZ2}$	$\overline{RRD} \uparrow$ to ADDRESS High Impedance (ADDRESS hold)	THMC1 - 10	THMC1 + 10 (THMC1)	ns
$t_{SHL1}$	ADDRESS valid to $\overline{RWR} \downarrow$ (ADDRESS setup)	THMC2 - 10 (THMC2 - 20)	THMC2 + 5 (THMC2)	ns
$t_{HLZ1}$	$\overline{RWR} \uparrow$ to DATA High Impedance (DATA hold)	THMC1 - 10 (THMC1 - 20)	THMC1 + 10 (THMC1)	ns
$t_{HLZ2}$	$\overline{RWR} \downarrow$ to ADDRESS High Impedance (ADDRESS hold)	THMC1 - 10 (THMC1 - 20)	THMC1 + 10 (THMC1)	ns
$t_{PW1}$	$\overline{RWR} \downarrow$ to $\overline{RWR} \uparrow$	MCLK - 10 (MCLK - 5)	MCLK + 5	ns
$t_{OOHL2}$	$\overline{DMAG} \downarrow$ to $\overline{STDINT} \uparrow$	8 x MCLK (8 x MCLK + 0.5)	13 x MCLK (10 x MCLK + 1)	ns
$t_{SLH1}$	DATA valid to $(\overline{WR} + \overline{CS}) \uparrow$ (DATA setup)	5 (60) <sup>1</sup>	--	ns

Notes:

1. Data sheet previously specified the data being valid to the rising edge of  $(\overline{WR} + \overline{CS})$ .

