

### UT80CXX196KD (JD02D) Pin 66 Function Change from XTAL2 to VSS

#### Abstract:

UTMC has performed a migration of the UT80C196KD and the UT80CRH196KD (PIC# JD02, SMD# [5962R98583](#)) from revision C to revision D. The following design bugs have necessitated the migration of the JD02C mask set to JD02D:

1. Title: [UT80CXX196KD \(JD02X\) HSO Timer2 Reset Interrupt Anomaly](#)  
URL: [http://www.utmc.com/products/80196\\_hstimer\\_err.pdf](http://www.utmc.com/products/80196_hstimer_err.pdf)
2. Title: [UT80CXX196KD \(JD02X\) NORML Instruction Operation](#)  
URL: [http://www.utmc.com/products/80196\\_norml\\_err.pdf](http://www.utmc.com/products/80196_norml_err.pdf)
3. Title: [UT80CXX196KD \(JD02X\) External Timer2 Reset Functionality](#)  
URL: [http://www.utmc.com/products/80196\\_exttimer\\_err.pdf](http://www.utmc.com/products/80196_exttimer_err.pdf)

During the migration, UTMC decided to change the functionality of pin 66 on the 68-pin ceramic quad flat pack. In all previous versions of the UT80CXX196KD, pin 66 was named XTAL2, and UTMC defined the pin as a no-connect that would always drive low. In the D revision of the UT80CXX196KD, UTMC has changed pin 66 to a VSS pin. UTMC decided to use this pin as a device ground pin in an attempt to reduce noise on the ALE signal. You can obtain the following application note regarding ALE noise on the UTMC web site. This application note is entitled:

[UT80CXX196KD Microcontroller Ale Considerations](#) located at [http://www.utmc.com/products/80196\\_ale\\_ap.pdf](http://www.utmc.com/products/80196_ale_ap.pdf)

#### Background:

The XTAL2 signal (pin 66) on the industry standard 8XC196KD is the inverted, fed-back copy of XTAL1 signal, and is output from the on-chip oscillator circuit within the microcontroller. When a digital oscillator is used to clock the microcontroller, the user must not connect the XTAL2 pin of the industry standard 8XC196KD. Because the UT80CXX196KD requires a digital oscillator, UTMC recommended that the user leave the XTAL2 pin unconnected although the controller did drive the pin low at all times. In the D revision of the UT80CXX196KD, UTMC changed the XTAL2 pin from a constant low drive output to a VSS power pin. By adding an additional ground pin to the UT80CXX196KD, the ALE signal does not glitch as badly as it does in previous versions of the microcontroller. This ALE glitch is caused by a large influx of current through the ground pins on the device when the ADDRESS/DATA bus and EDAC check bits switch from all high to all low. This typically occurs after the falling edge of the ALE signal when the microcontroller drives data onto the bus after supplying a valid address during a write operation. Therefore, a second low-high-low glitch on the ALE signal could cause the address latch to change the address information.

Because the original description of the XTAL2 pin for revisions A, B, and C of the UT80CXX196KD defines that the pin is always driven low, any design that uses this device should not be affected by the function change. If a design had anything tied to the XTAL2 pin, the designer would anticipate that the XTAL2 signal always drives low, similar to shorting a signal to ground. However, in order to help alleviate noise on the ALE pin, a design using the UT80CXX196KD revision D microcontroller should short pin 66 to the VSS plane. If an existing design can not be modified to short pin 66 to ground on the revision D microcontroller, then it should be left unconnected, however, UTMC can not guarantee the ALE noise reduction. Further, all designs using the UT80CXX196KD should consider the possible ALE noise mitigation solutions that are defined in the above listed application note.

To help all user's of the UT80CXX196KD anticipate the function change of pin 66, UTMC has updated the datasheet and SMD by replacing all occurrences of XTAL2 with a VSS description, and the difference to the industry standard 8XC196KD has been included in Appendix A of the datasheet.