Standard Products

RAD1419 Analog-to-Digital Converter

Data Sheet

January, 2012
www.aeroflex.com/AtoD

FEATURES

- 800ksps sample rate
- 150mW power dissipation
- Typical performance: 81.5dB S/(N + D) and 93dB THD
- No missing pipeline delays or missing codes
- Nap and shutdown modes
- Operates with 2.5V internal 15ppm/^{o}C reference or external reference
- True differential inputs reject common mode noise
- 20MHz full-power bandwidth sampling
- Bipolar input range: ±2.5V
- Operational Environment; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 100 krad(Si)
  - Latchup immune (LET ≤ 55 MeV-cm^2/mg)
- Packaging options:
  - 28-lead hermetic ceramic flatpack
- Class S A-to-D Converter built to your custom flow

INTRODUCTION

Aeroflex RAD's RAD1419 Analog-to-Digital Converter (ADC) is a 1µs, 800ksps, 14-bit sampling A/D converter that draws only 150mW from ±5V supplies. This easy-to-use device includes a high dynamic range sample-and-hold and a precision reference. Two digitally selectable power shutdown modes provide flexibility for low power systems.

The RAD1419 has a full-scale input range of ±2.5V. Outstanding AC performance includes 81.5dB S/(N + D) and 93dB THD with a 100kHz input; 80dB S/(N + D) and 86dB THD at the Nyquist input frequency of 400kHz.

The unique differential input sample-and-hold can acquire single-ended or differential input signals up to its 20MHz bandwidth. The 60dB common mode rejection allows users to eliminate ground loops and common mode noise by measuring signals differentially from the source.

The ADC has a ìP compatible, 14-bit parallel output port. There is no pipeline delay in the conversion results. A separate convert start input and data ready signal (BUSY) ease connections to FIFOs, DPSs and microprocessors.

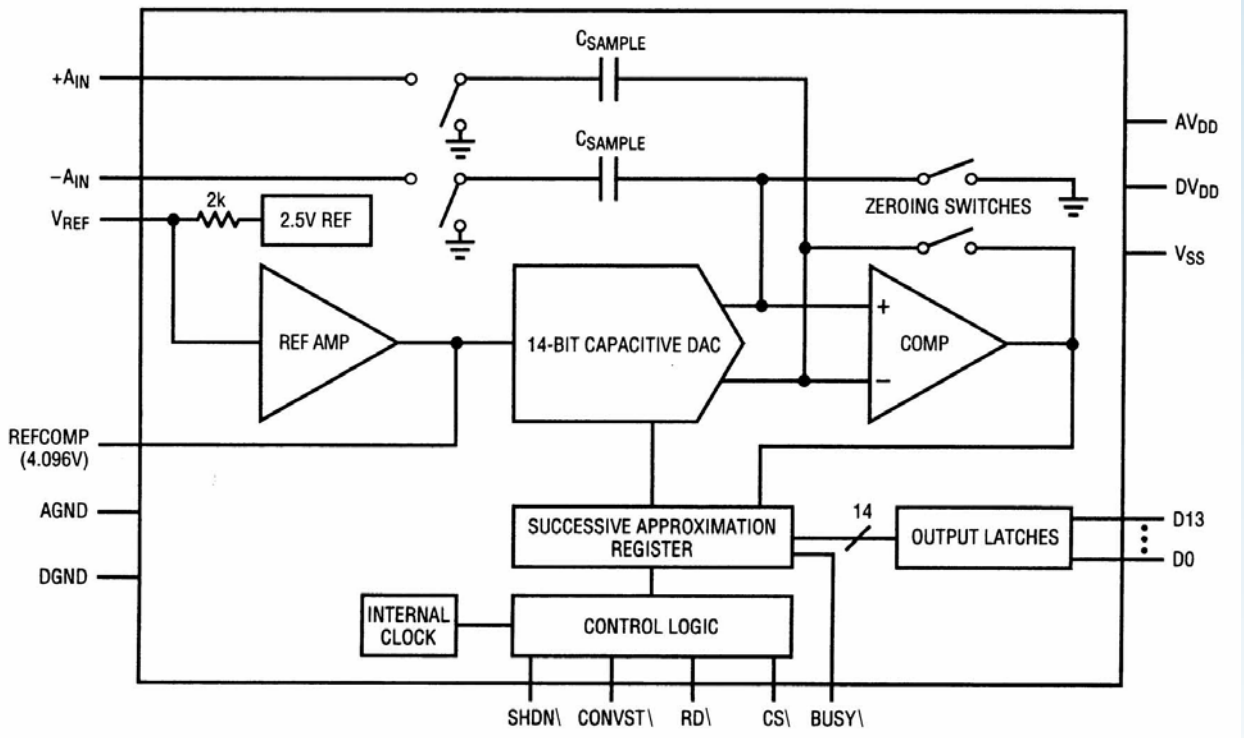


Figure 1. RAD1419 Block Diagram

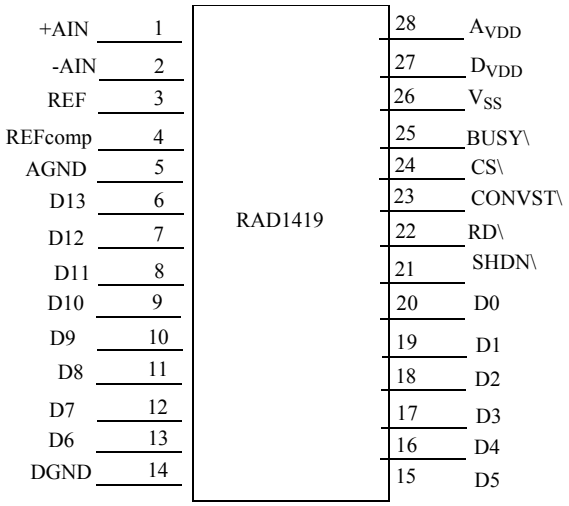


Figure 2. RAD1419 Pinout

PIN DESCRIPTION

Pin Name	I/O	No.	Description
+AIN		**1**	±2.5V Positive analog input
-AIN		**2**	±2.5V Negative analog input
VREF		**3**	2.5V Reference output. Bypass to AGND with 1µF.
REFcomp		**4**	4.06V Reference output. Bypass to AGND with 10µF.tantalum in parallel with 0.1µF.or 10µF ceramic.
AGND		**5**	Analog ground
D13 to D6		**6-13**	Three-state data outputs. The output format is 2's complement.
DGND		**14**	Digital ground for internal logic. Tie to AGND.
D5 to D0		**0-5**	Three-state data outputs. The output format is 2's complement.
SHDN		**21**	Power shutdown input. Low selects shutdown. Shutdown mode selected by CS\. CS\ = 0 nap mode and CS\ = 1 for sleep mode.
RD		**22**	Read input. This enables the output drivers when CS\ is low.
CONVST		**23**	Conversion start signal. This active low signal starts a conversion on its falling edge.
CS		**24**	Chip select. The input must be low for the ADC to recognize CONVST\ and RD\ inputs. CS\ also sets the shutdown mode when SHDN\ goes low. CS\ and SHDN\ low select the quick wake-up nap mode. CS\ high and SHDN\ low select sleep mode.
BUSY		**25**	The BUSY\ output shows the converter status. It is low when a conversion is in progress. Data valid on the rising edge of BUSY\.
V_{SS}		**26**	5V Negative supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF.or 10µF ceramic.
D_{VDD}		**27**	5V Positive supply. Short to Pin 28.
A_{VDD}		**28**	5V Positive Supply. Bypass to AGND with10µF tantalum in parallel with 0.1µF.or 10µF ceramic.

OPERATIONAL ENVIRONMENT

PARAMETER	LIMIT	UNITS
Total Ionizing Dose (TID)	1.0E5	rad(Si)
Single Event Latchup (SEL)	≤55	MeV-cm^2/mg
Neutron Fluence[1]	1.0E13	n/cm^2

Notes:
1. Guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS[1]
(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	Supply voltage	6.0V
V_{SS}	Negative supply voltage	-6V
V_{DD} to V_{SS}	Total supply voltage	12V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	500mW
T_J	Maximum junction temperature	TBD
Θ_{JC}	Thermal resistance, junction-to-case[2]	TBD

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{SS} to V_{DD}	Input/output voltage	-0.5V to +0.5V
T_C	Case temperature range	-55 to +125°C

ELECTRICAL CHARACTERISTICS

CONVERTER CHARACTERISTICS

*Denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = +25°C. With Internal Reference.[5,6]

SYMBOL	PARAMETER	CONDITIONS	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
	Resolution	(No Missing Codes)	1 2 3	14			Bits
INL	Integral Linearity Error	Note 7/	1 2 3		±0.8	±2	LSB
DNL	Differential Linearity Error		1 2 3		±0.7 ±0.7	±1.5 ±2	LSB LSB
	Offset Error	Note 8/	1 2 3		±5	±20	LSB
	Full scale Error Internal Reference		1		±10	±60	LSB
	Full scale Error ExternalReference	2.5V			±5		LSB
	Full Scale Tempco	I_{OUT}(REF) = 0			±15		ppm/°C

ANALOG INPUT

*Denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = +25°C.[5]

SYMBOL	PARAMETER	CONDITIONS	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range	4.75V ≤ V_{DD} ≤ 5.25V, -5.25V ≤ V_{SS} ≤ -4.75V *			±2.5		V
I_{IN}	Analog Input Leakage Current	CS\ = HIGH	1 2 3			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions			15		pF
C_{IN}	Analog Input Capacitance	During Conversions			5		pF
t_{ACQ}	Sample-and-Hold Acquisition Time	Note 9/			90	300	ns
t_{AP}	Sample-and-Hold Aperture Delay Time				-1.5		ns
t_{JITTER}	Sample-and-Hold Aperture Delay Time Jitter				2		psRMS
CMRR	Analog Input Common Mode Rejection Ratio	-2.5V < (-AIN = AIN) < 2.5V			60		dB

DYNAMIC ACCURACY

*Denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = +25°C.[5]

SYMBOL	PARAMETER	CONDITIONS	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to (Noise + Distortion) Ratio	100 KHz Input Signal *	4	78	81.5		dB
S/(N + D)	Signal-to (Noise + Distortion) Ratio	390 KHz Input Signal *			80.0		dB
THD	Total Harmonic Distortion	100 KHz Input Signal, First 5 Harmonics *	4		-93	-86	dB
THD	Total Harmonic Distortion	390 KHz Input Signal, First 5 Harmonics *			-86		dB
SFDR	Spurious Free Dynamic Range	100 KHz Input Signal *	4		-95	-86	dB
IMD	Intermodulation Distortion	$f_{IN}1$ = 29.37 KHz, $f_{IN}2$ = 32.446 KHz			-86		dB
	Full-Power Bandwidth				20		MHz
	Full-Linear Bandwidth	S/(N + D) $\geq$ 77dB			1		MHz

INTERNAL REFERENCE CHARACTERISTICS[5]

SYMBOL	PARAMETER	CONDITIONS	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
V_{REF}	Output Voltage	I_{OUT} = 0	1 2 3	2.480	2.500	2.520	V
V_{REF}	Output Tempco	I_{OUT} = 0			±15		ppm/°C
V_{REF}	Line Regulation	4.75V < V_{DD} < 5.25V, -5.25V < V_{SS} < -4.75V			0.05		LSB/V
V_{REF}	Output Resistance	-0.1mA < | I_{OUT} | < 0.1mA			2		kΩ
REFCOMP	Output Voltage	I_{OUT} = 0			4.06		V

DIGITAL INPUTS AND DIGITAL OUTPUTS

*Denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = +25°C.[5]

SYMBOL	TEST	TEST CONDITION	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V * Note 12	1 2 3	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V * Note 12	1 2 3			**0.8**	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD} *	1 2 3			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V IO = -10µA*			4.5		V
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V IO = -200µA	1 2 3	4.0			V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V IO = 160µA			0.05		V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V IO = 1.6mA *	1 2 3		0.10	0.4	V
I_{OZ}	High-Z Output Leakage D13 to D0	V_{OUT} = 0V to V_{DD}, CS\ High *	1 2 3			±10	µA
C_{OZ}	High-Z Output Capacitance D13 to D0	CS\ High, Note 9/ *				15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			-10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS

Denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = +25°C.[5]

SYMBOL	PARAMETER	CONDITIONS	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	Note 10/		4.75		5.25	V
V_{SS}	Negative Supply Voltage	Note 10/		-4.75		-5.25	V
I_{DD}	Positive Supply Current		1 2 3		11	20	mA
I_{DD}	Positive Supply Current	Nap Mode: SHDN\ = 0V, CS\ = 0V			1.5		mA
I_{DD}	Positive Supply Current	Sleep Mode: SHDN\ = 0V, CS\ = 5V			250		µA
I_{SS}	Negative Supply Current		1 2 3		19	30	mA
I_{SS}	Negative Supply Current	Nap Mode: SHDN\ = 0V, CS\ = 0V			100		µA
I_{SS}	Negative Supply Current	Sleep Mode: SHDN\ = 0V, CS\ = 5V			1		µA
P_{DIS}	Power Dissipation		1 2 3		150	240	mW
P_{DIS}	Power Dissipation	Nap Mode: SHDN\ = 0V, CS\ = 0V	1 2 3		7.5	1.2	mW
P_{DIS}	Power Dissipation	Sleep Mode: SHDN\ = 0V, CS\ = 5V			1.2		mW

TIMING CHARACTERISTICS

*Denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = +25°C.[5]

SYMBOL	PARAMETER	CONDITIONS	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
f_{SAMPLE} (MAX)	Maximum Sampling Frequency	Note 9/ *	9 10 11	800			kHz
t_{CONV}	Conversion Time		9 10 11		950	1150	ns
t_{ACQ}	Acquisition Time	Note 9/ *	9 10 11		90	300	ns
t_{ACQ} + CONV	Acquisition + Conversion Time	Note 9/ *	9 10 11		1040	1250	ns
t_1	CS\ to RD\ Setup Time	Note 9/ *		0			ns
t_2	CS\ to CONVST\ Setup Time	Note 9/ *		40			ns
t_3	CS\ to SHDN\ Setup Time	Note 9/		40			ns
t_4	SHDN\ to CONVST\ Wake-up Time	Note 10/			400		ns
t_5	CONVST\ Low Time	Notes 9/,11/ *	9 10 11	40			ns
t_6	CONVST\ to BUSY\ Delay	CL = 25pF	9		20		ns
t_6	CONVST\ to BUSY\ Delay	CL = 25pF	9 10 11			50	ns
t_7	Data Ready Before BUSY\		9	20	50		ns
t_7	Data Ready Before BUSY\	Note 9/	9 10 11	15			ns
t_8	Delay Between Conversions	Note 9/ *	9 10 11	40			ns
t_9	Wait Time RD\ After BUSY\	Note 9/ *		-5			ns
t_{10}	Data Access Time After RD\	CL = 25pF	9		15	25	ns
t_{10}	Data Access Time After RD\	CL = 25pF, Note 9/	9 10 11			35	ns
t_{10}	Data Access Time After RD\	CL = 100pF, Note 9/	9		20	35	ns
t_{10}	Data Access Time After RD\	CL = 100pF, Note 9/	9 10 11			50	ns
t_{11}	Bus Relinquish Time	Note 9/	9		10	20	ns

TIMING CHARACTERISTICS (Cont'd)

*Denotes specifications which apply over the full operating temperature range, otherwise specifications are TA = +25°C.[5]

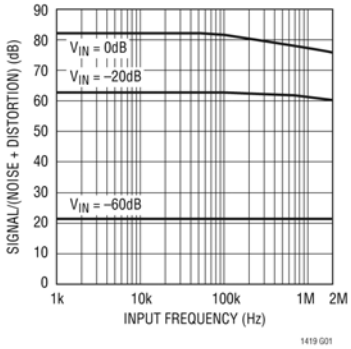
SYMBOL	PARAMETER	CONDITIONS	GROUP A SUBGROUPS	MIN	TYP	MAX	UNITS
t_{11}	Bus Relinquish Time		9			35	ns
			10				
RD\ Low Time	t_{12}	Note 9/ *	9	t10			ns
			10				
			11				
CONVST\ High Time	t_{13}	Note 9/ *	9	40			ns
			10				
			11				
			11				

Notes:

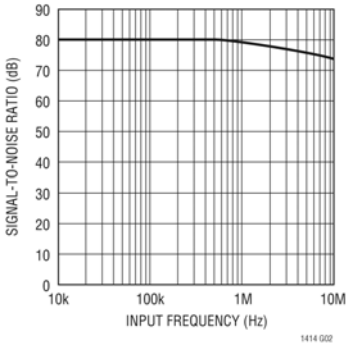
Parameters listed only as "Typical" are not tested in production.

1. Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
2. All voltage values are with respect to ground with D_{GND} and A_{GND} wired together unless otherwise noted.
3. When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{DD} without latch up.
4. When these pin voltages are taken below V_{SS}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latch up. These pins are not clamped to V_{DD}.
5. V_{DD} = 5V, V_{SS} = -5V, f_{SAMPLE} = 800kHz, tr = tf = 5ns unless otherwise specified.
6. Linearity, offset and full-scale specifications apply for a single ended $+A_{IN}$ input with - A_{IN} grounded.
7. Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.
8. Bipolar offset is the offset voltage measured from -0.5LSB when the output code flickers between 0000 0000 0000 00 and 1111 1111 1111 11.
9. Guaranteed by design or characterization, not subject to test in production.
10. Recommended operating conditions.
11. The falling edge of CONVST\ starts a conversion. If CONVST\ returns high at a critical point during the conversion it can create small errors. For best performance ensure that CONVST\ returns high either within 650ns after the start of the conversion
12. V_{IH} and V_{IL} will be guaranteed by testing V_{OH} and V_{OL} at the appropriate levels.

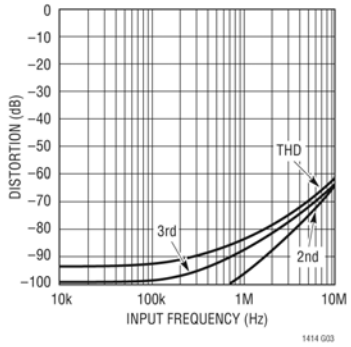
S/(N+D) vs Input Frequency and Amplitude



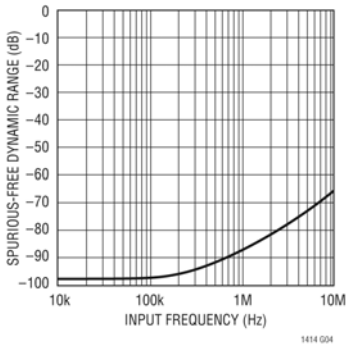
Signal-to-Noise Ratio



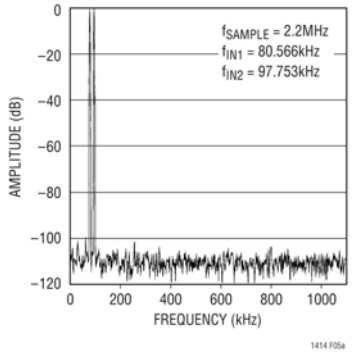
Distortion vs Input Frequency



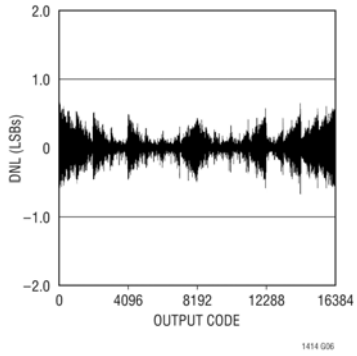
Spurious-Free Dynamic Range vs Input Frequency



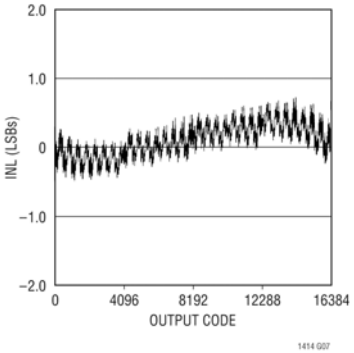
Intermodulation Distortion Plot



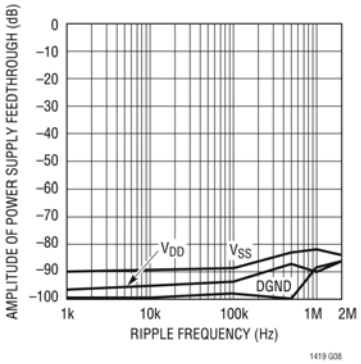
Differential Nonlinearity vs Output Code



Integral Nonlinearity vs Output Code



Power Supply Feedthrough vs Ripple Frequency



Input Common Mode Rejection vs Input Frequency

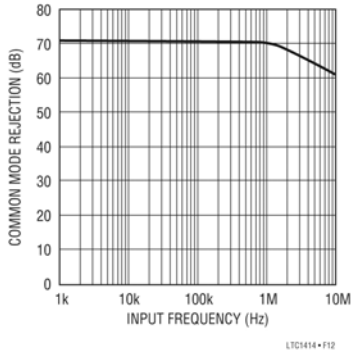


Figure 2. Typical Performance Characteristics

ELECTRICAL REQUIREMENTS

TEST REQUIREMENTS	SUBGROUPS
Pre Burn-in electrical parameters	1,4,9
Interim electrical parameters	1,4,9
Final electrical test parameters	1,2,3,4,9,10,11
Post seal electrical test parameters	1
Group A electrical test parameters	1,2,3,4,9,10,11
Group B electrical test parameters	1,4,9
Group C electrical test parameters	1,4,9
Group D electrical test parameters	1,4,9

SUBGROUPS	Definitions
1	Static characteristics 25^{o}C
2	Static characteristics 125^{o}C
3	Static characteristics -55^{o}C
4	Static characteristics 25^{o}C
5	Static characteristics 125^{o}C
6	Static characteristics -55^{o}C
9	Static characteristics 25^{o}C
10	Static characteristics 125^{o}C
11	Static characteristics -55^{o}C

PACKAGING

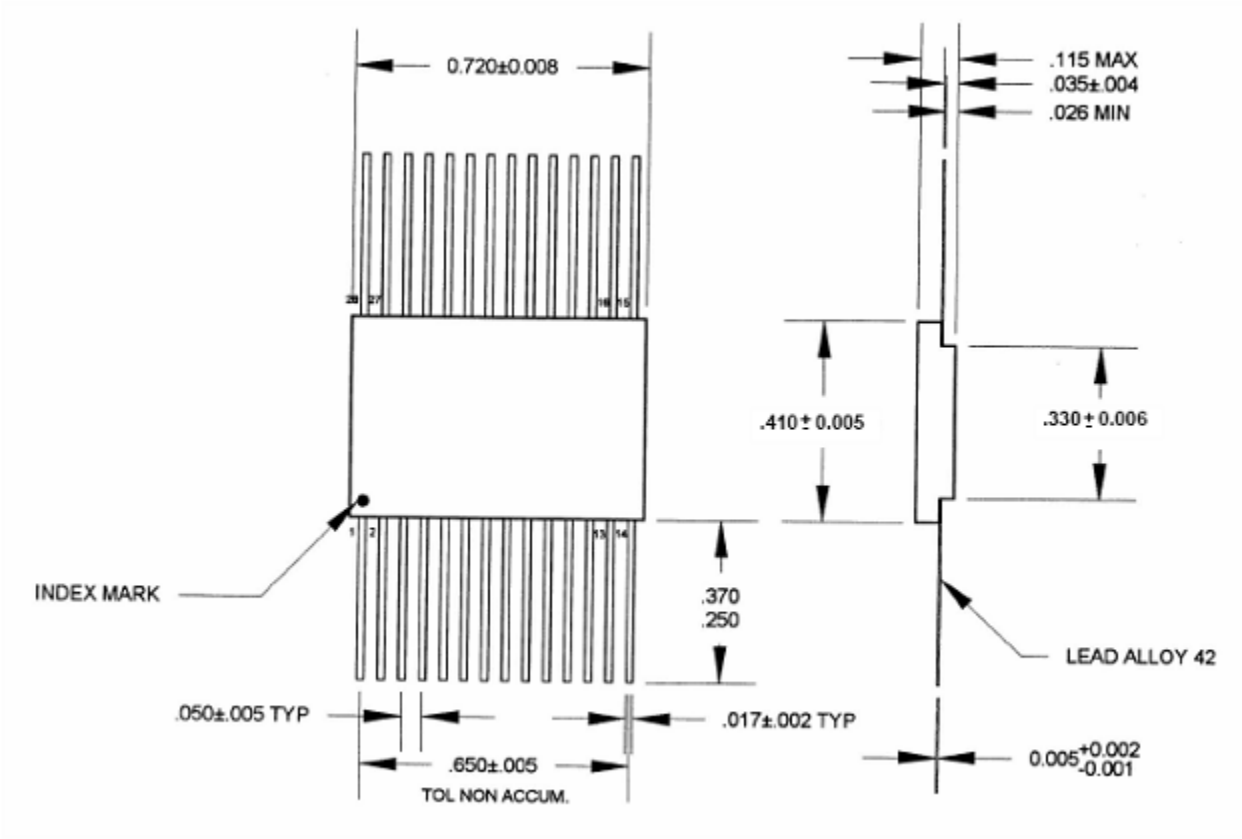
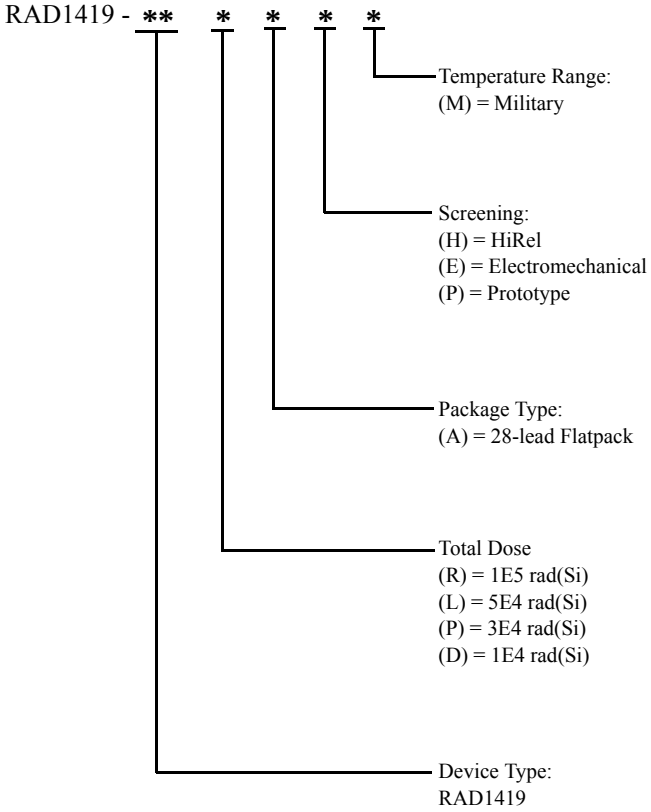


Figure 4. 28-Lead Hermetic Ceramic Flatpack

ORDERING INFORMATION

RAD1419:



Notes:

1. Military temperature range: -55°C to 125°C.

2. Prototype devices are tested at 25°C only, in a production package.

3. Electromechanical devices are tri-temp tested (-55°C, 25°C, 125°C), post-assembly screening: fine and gross leak, burn-in a production package.

Datasheet - Class S Compliant

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