

QCOTS™ UT8SDSQ128M8 1 Gigabit SDRAM

Product Brief
March 25, 2004



FEATURES

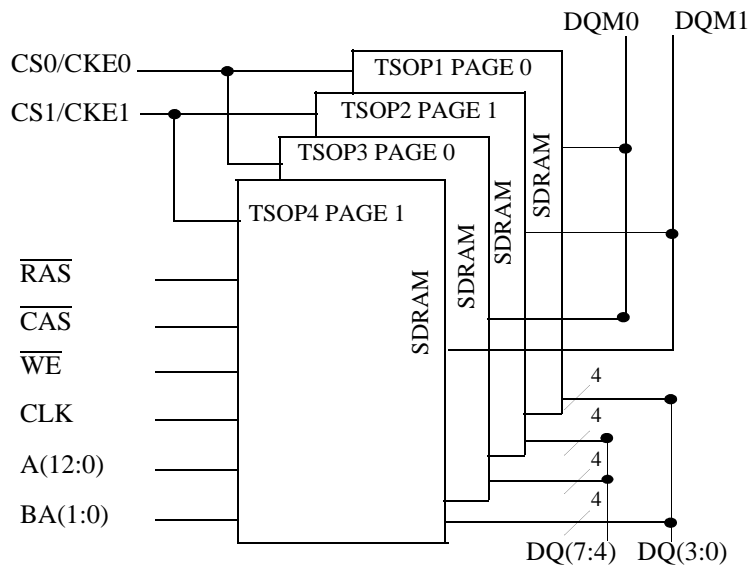
- ❑ Organized 128M x 8bits
- ❑ Single JEDEC standard 3.3V power supply
- ❑ 33MHz operation -40°C to 85°C
- ❑ LVTTTL compatible with multiplexed address
- ❑ Four bank operation
- ❑ MRS cycle with address key program
 - CAS latency (2 and 3)
 - Burst length (8)
 - Burst type (sequential and interleave)
- ❑ Fully synchronous; all signals registered on positive edge of system clock
- ❑ Burst read single-bit write operation
- ❑ Auto-refresh and self-refresh
- ❑ Typical radiation performance
 - Total dose > 10krad(Si)
 - SEL Immune >40-60 MeV-cm²/mg (contact factory)
- ❑ Package options:
 - 54-lead Small Outline Package (SOP)
- ❑ Max temperature at module side during installation should not exceed 215°C

INTRODUCTION

The UT8SDSQ128M8 is a high performance, highly integrated Synchronous Dynamic Random Access Memory (SDRAM) stack. Total module density is 1,073,741, 824 bits of storage. Organization is two (2) pages of 512 Mbits. Each memory page is organized 64M by 8 bits (pages are organized as four (4) banks of 16M x 8 selected via BA(1:0)). The two pages have an 8-bit interface independently selectable using the appropriate active-low chip select pin (\overline{CS}_n). All other signals are common to the four (4) 256 Mbit SDRAM memories.

Synchronous design allows precise memory accesses through the use of two system clocks. This architecture provides the ability for I/O transactions being performed on the positive edge of each clock cycle.

Ideal uses for the UT8SDSQ128M8 include space applications requiring high performance and high density, such as a space borne solid state recorder. In addition, the programmable burst length and programmable \overline{CAS} latencies enable the device to be used in a variety of high bandwidth space applications.



Common Signals: \overline{RAS} , \overline{CAS} , \overline{WE} , CLK, A(12:0) and BA(1:0)

Figure 1: UT8SDSQ128M8 Functional Block Diagram (1Gb STACK)