

Standard Products

ACT4469D Dual Variable Amplitude Transceiver for H009 Specification

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FEATURES

- World's smallest and lowest standby power dual variable amplitude H009 transceiver 1.25" x 0.61" maximum ceramic package
- Dual transceiver with variable output amplitude control meets McDonnell Douglas H009 data bus specifications
- Lowest standby power
- Low power dissipation at full output power
- Operates with $\pm 12V$ to ± 15 and $+5V$ power supplies
- Monolithic construction using linear ASICs
- $+10V$ Control line for transmitter amplitude adjustment (See Figure 3)
- Packaging – Hermetic Ceramic
 - Non-conductive mounting surface
 - No package glass beads
 - Small size & light weight
- Designed for commercial, industrial and aerospace applications
- Aeroflex is a Class H & K MIL-PRF-38534 Manufacturer

DESCRIPTION

The Aeroflex Plainview transceiver model ACT4469D is a new generation monolithic transceiver which provides variable amplitude in compliance with H009 data bus requirements with the lowest standby power consumption available using three DC power supplies operation. The dual channel ACT4469D performs the front-end analog function of inputting and outputting data through a transformer to a H009 data bus.

Design of these transceivers reflects particular attention to active filter performance. This results in low bit and word error rate with superior waveform purity and minimal zero crossover distortion. The active filter design provides the required H009 low harmonic distortion waveform without increasing the pulse delay characteristics significantly. Efficient transmitter electrical and thermal design provides low internal power dissipation and heat rise at high and well as low duty cycles.

The receiver input threshold is set internally. Variable amplitude is adjusted with factory preset 0 – 10VDC control line at 2mA maximum input current at 10Volts.

TRANSMITTER

The Transmitter section accepts complementary TTL data at the input, and when coupled to the data bus with a 1:1 transformer, isolated on the transceiver side with two 34 Ohm bus terminating resistors, with the bus terminated by a 175 Ohm resistor, the data bus signal produced is 20VP-P nominal at A-A' (See Figure 5). When both DATA and $\overline{\text{DATA}}$ inputs are held low or high, the transmitter output becomes a low impedance and signal is "removed" from the line. In addition, an overriding "INHIBIT" input returns the output to a high impedance state. A logic "1" applied to the "INHIBIT" takes priority over the condition of the data inputs and disables the transmitter (See Transmitter Logic Waveforms - Figure 1).

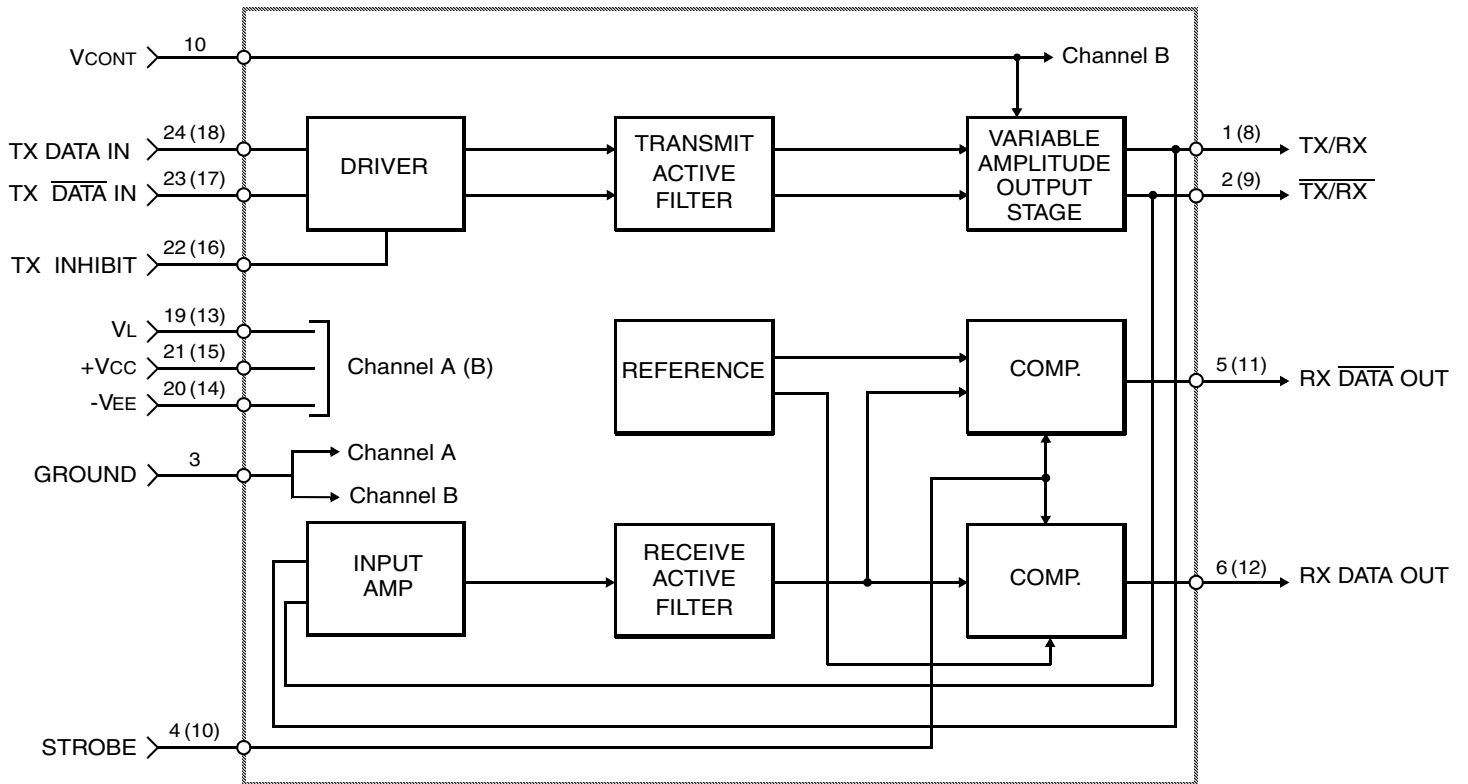
The transmitter utilizes an active filter to suppress harmonics above 1 MHz to meet H009 specifications. The transmitter may be safely operated for an indefinite period at 100% duty cycle into a data bus short circuit.

RECEIVER

The Receiver section accepts bi-phase differential data at the input and produces two TTL signals at the output. The outputs are DATA and $\overline{\text{DATA}}$, and represent positive and negative excursions of the input beyond a pre-determined threshold (See Receiver Logic Waveforms - Figure 2).

The internal threshold is nominally set to detect data bus signals exceeding 1.0VP-P and reject signals less than 0.6VP-P when used with a 1:1 turns ratio transformer (See Figure 5 for transformer data and typical connection).

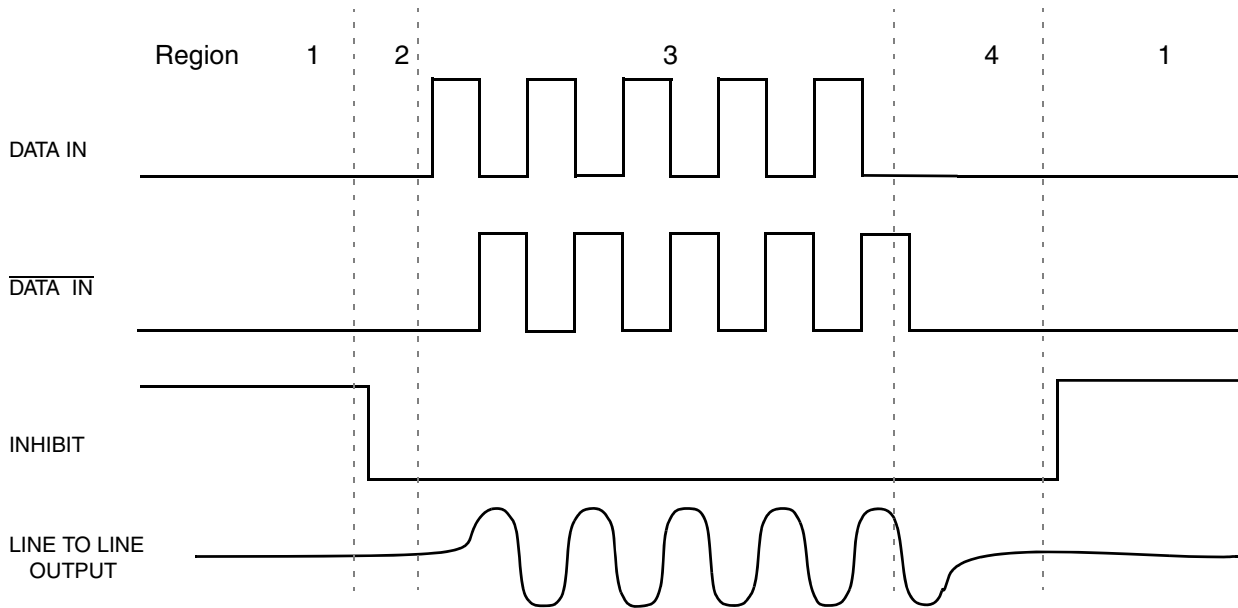
A low level at the Strobe input inhibits the DATA and $\overline{\text{DATA}}$ outputs. If unused, a 2K Ohm pull-up to +5VDC is recommended.



**BLOCK DIAGRAM
(WITHOUT TRANSFORMER, CHANNEL A SHOWN)
CHANNEL A (CHANNEL B)**

DATA	$\overline{\text{DATA}}$	INHIBIT	OUTPUT
X	X	H	High Z
H	H	L	Low Z (No signal)
L	L	L	
H	L	L	Low Z (Signal)
L	H	L	

FIGURE 1A – TX OUTPUT TRUTH TABLE



- Notes: 1. Data and $\overline{\text{DATA}}$ inputs must be complementary waveforms or 50% duty cycle average, with no delays between them, and in the same state during the off time (both high and low).
 2. **Region 1;** no output signal, High Z state, (Receive Mode), **Region 2;** No Output signal, Low Z state, **Region 3;** Transmitter signal on, low Z (Transmitter mode), **Region 4;** No Output signal, Low Z state, (Terminate Mode).

FIGURE 1A – TRANSMITTER LOGIC WAVEFORMS

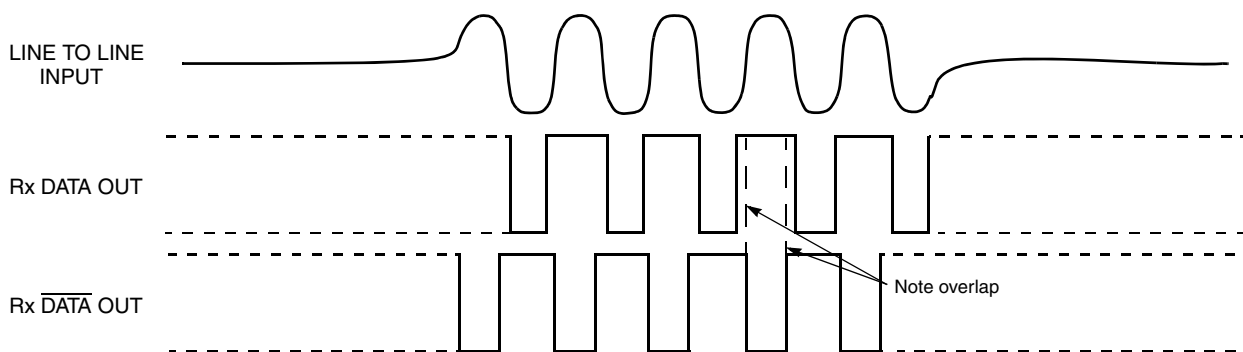


FIGURE 2 – RECEIVER LOGIC WAVEFORMS

ABSOLUTE MAXIMUM RATINGS

Operating Case Temperature	-55°C to +125°C	
Storage Case Temperature	-65°C to +150°C	
Power Supply Voltages	±18 V	+7 V
Logic Input Voltage	-0.3 V to +5.5 V	
Receiver Differential Input	±40 V	
Receiver Input Voltage (Common Mode)	±10V	
Driver Peak Output Current	150 mA	
Total Package Power Dissipation over the Full Operating Case Temperature Range	3.6 Watts	
Maximum Junction to Case Temperature (100% duty cycle)	18°C	
Junction-Case, Thermal Resistance	5°C/W	

ELECTRICAL CHARACTERISTICS – DRIVER SECTION 1/ 2/

INPUT CHARACTERISTICS, TX DATA IN OR TX DATA IN

Parameter	Condition	Symbol	Min	Typ	Max	Unit
"0" Input Current	$V_{IN} = 0.4V$	I_{ILD}	-	-0.2	-0.4	mA
"1" Input Current	$V_{IN} = 2.7V$	I_{IHD}	-	1	40	μA
"0" Input Voltage	-	V_{ILD}	-	-	0.7	V
"1" Input Voltage	-	V_{IHD}	2.0	-	-	V

INHIBIT CHARACTERISTICS

"0" Input Current	$V_{IN} = 0.4V$	I_{ILI}	-	-0.2	-0.4	mA
"1" Input Current	$V_{IN} = 2.7V$	I_{IHI}	-	1.0	40	μA
"0" Input Voltage	-	V_{ILI}	-	-	0.7	V
"1" Input Voltage	-	V_{IHI}	2	-	-	V
Delay from TX inhibit, (0→1) to inhibited output	-	t_{DXOFF}	-	300	500	nS
Delay from TX inhibit, (1→0) to active output	-	t_{DXON}	-	200	400	nS
Differential Output Noise, inhibit mode	-	V_{NOI}	-	2	10	mVp-p
Differential Output Impedance (inhibited)	4/	Z_{OI}	10K	-	-	Ω

OUTPUT CHARACTERISTICS

Differential output level (175Ω)	Point A - A'	V_O	16	20	24	V p-p
Rise and Fall Times (10% to 90% of p-p output)	-	t_R & t_F	200	260	300	nS
Output Offset, Figure4 5/	Point A - A'	V_{OS}	-	-	±260	mV peak
Delay from 50% point of TX DATA or TX DATA input to zero crossing of differential signal (Note 1)	-	t_{DTX}	-	280	400	nS
Control Line Input Resistance 3/	-	RCONT	5	-	-	KΩ

ELECTRICAL CHARACTERISTICS – RECEIVER SECTION 1/ 2/

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Differential Voltage Range 3/	Point A-A'	V_{IDR}	-	-	20	V _{PEAK}
Common Mode Rejection Ratio 3/	-	CMRR	45	-	-	dB

STROBE CHARACTERISTICS (Logic '0' Inhibits Output) (NOTE: If not used, a 1K pullup to 5V is recommended)

"0" Input Current	$V_S = 0.4V$	I_{IL}	-	-0.2	-0.4	mA
"1" Input Current	$V_S = 2.7V$	I_{IH}	-	1	+40	μA
"0" Input Voltage	-	V_{IL}	-	-	0.7	V
"1" Input Voltage	-	V_{IH}	2.0	-	-	V
Strobe Delay (turn-on or turn-off)	-	$t_{SD(ON/OFF)}$	-	90	150	nS

THRESHOLD CHARACTERISTICS (Sinewave Input)

Internal Threshold Voltage, Point A-A' Figure 5	1MHz	V_{TH}	1.5	2.0	3.0	V _{P-P}
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OUTPUT CHARACTERISTICS, RX DATA AND RX DATA

"1" State	$I_{OH} = -0.4mA$	V_{OH}	2.5	3.6	-	V
"0" State	$I_{OL} = 4mA$	V_{OL}	-	0.35	0.5	V
Delay, (average) from differential input zero crossings to RX DATA and RX DATA output	6/ 50% points	t_{DRX}	-	300	450	nS

POWER SUPPLY CURRENT PER CHANNEL 1/ 2/

$V_{CC} = +12V$ to $+15V$, $V_{EE} = -12V$ to $-15V$, $V_L = +5V$

Duty Cycle	Condition	Symbol	Typ	Max	Unit
Transmitter Standby	Point A - A' $Z_O = 175\Omega$, $V_O = 21V_{P-P}$ Figure 5	I_{CC}	6	10	mA
		I_{EE}	15	25	
		I_L	22	30	
25%		I_{CC}	25	35	
		I_{EE}	36	45	
		I_L	22	30	
50%		I_{CC}	34	45	
		I_{EE}	45	55	
		I_L	22	30	
100%		I_{CC}	49	60	
		I_{EE}	60	70	
		I_L	22	30	

Notes:

- $V_{CC} = +15V$ to $\pm 0.75V$, $V_{EE} = -15V$ to $\pm 0.75V$, $V_{IL} = +5V$ to $\pm 0.5V$, $T_c = -55^\circ C$ to $+125^\circ C$, unless otherwise specified.
- All typical values are measured at $+25^\circ C$.
- Characteristics guaranteed by design, not production tested.
- Power ON/OFF, measured 1MHz at Point A-A' Figure 4.
- At point A-A' on Figure 4 or 5, 2.5 μS after midpoint crossing of the parity bit of the last word.
- This test is performed while the Transceiver is reading its own transmission. This condition is called "Wraparound". Standard TTL loads applied to RX DATA Outputs.

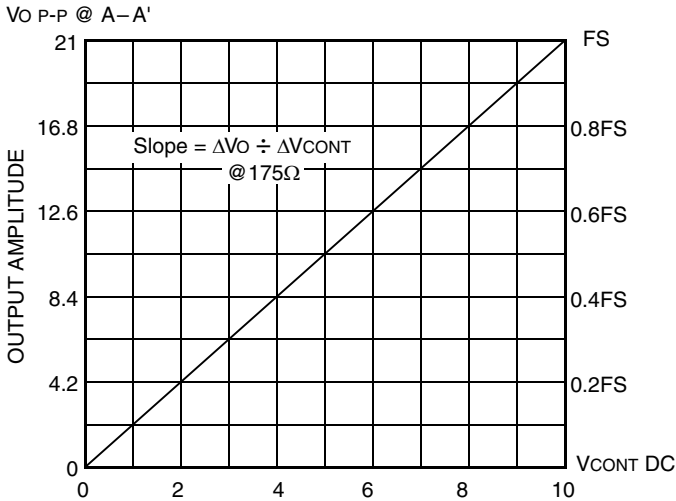
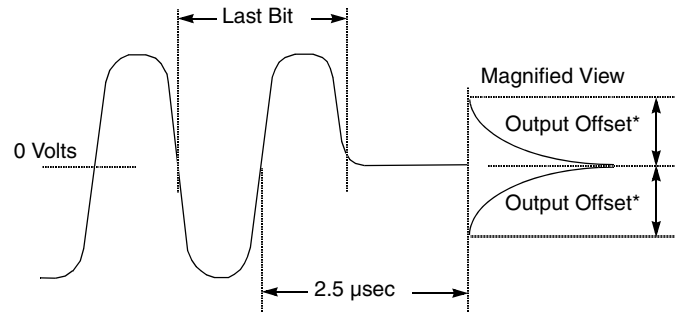
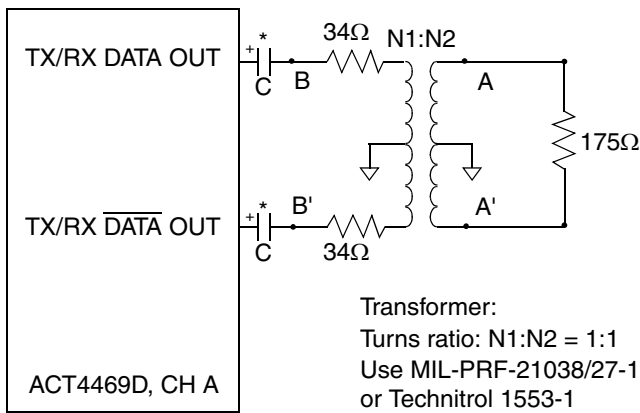


FIGURE 3 – TYPICAL TRANSMITTER OUTPUT AMPLITUDE (Vo) vs VCONT VOLTAGE



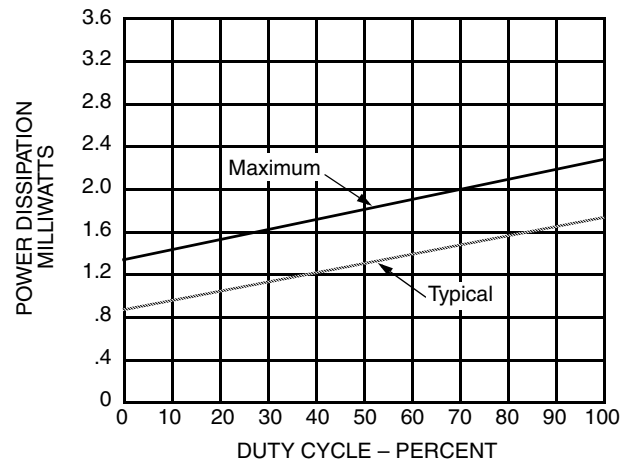
*Offset measured at point A-A' in Figure 5

FIGURE 4 – TRANSMITTER (TX) OUTPUT OFFSET



* External Coupling Capacitors are required for each output. Recommended 1μF ceramic 25V/50V or can use Tantalum.

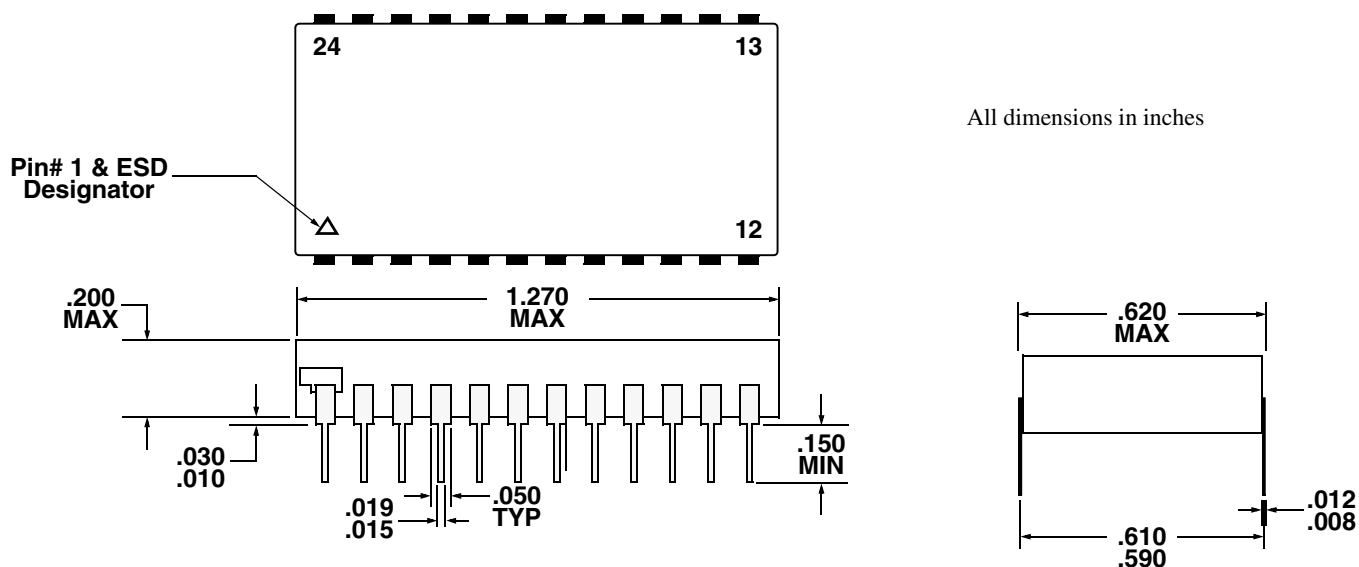
FIGURE 5 – TYPICAL TRANSFORMER CONNECTION



Note: Vcc = +15VDC, VEE = -15VDC, VBUS (Point A-A') at 21VP-P

FIGURE 6 – PACKAGE (PWRIN - PWRLOAD) POWER DISSIPATION vs DUTY CYCLE (Total Hybrid with one channel transmitting and the other in standby)

PACKAGE DIMENSIONS



PIN vs FUNCTION TABLE

Pin #	Function	Pin #	Function
1	TX DATA OUT A / RX DATA IN A	13	+5V B
2	TX $\overline{\text{DATA}}$ OUT A / RX $\overline{\text{DATA}}$ IN A	14	-15V B
3	GROUND	15	+15V B
4	STROBE A	16	INHIBIT B
5	RX DATA OUT A	17	TX $\overline{\text{DATA}}$ IN B
6	RX $\overline{\text{DATA}}$ OUT A	18	TX DATA IN B
7	10V CONTROL IN	19	+5V A
8	TX DATA OUT B / RX DATA IN B	20	-15V A
9	TX $\overline{\text{DATA}}$ OUT B / RX $\overline{\text{DATA}}$ IN B	21	+15V A
10	STROBE B	22	INHIBIT A
11	RX DATA OUT B	23	TX $\overline{\text{DATA}}$ IN A
12	RX $\overline{\text{DATA}}$ OUT B	24	TX DATA IN A

CONFIGURATIONS AND ORDERING INFORMATION

Model No.	Screening	DSCC SMD	Receiver Data level	Case
ACT4469-D	Military Temperature, -55°C to +125°C Screened in accordance with MIL-PRF-38534, Class H	Pending	Normally Low	DIP
ACT4469-DI			Normally High	
ACT 4469-D-7	Commercial flow, +25°C testing only	NA	Normally Low	
ACT 4469-DI-7			Normally High	

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