

Standard Products
CT2577 / CT2579
Remote Terminal & Bus Controller
 for MIL-STD-1553 / 1760 & McAir

www.aeroflex.com/Avionics

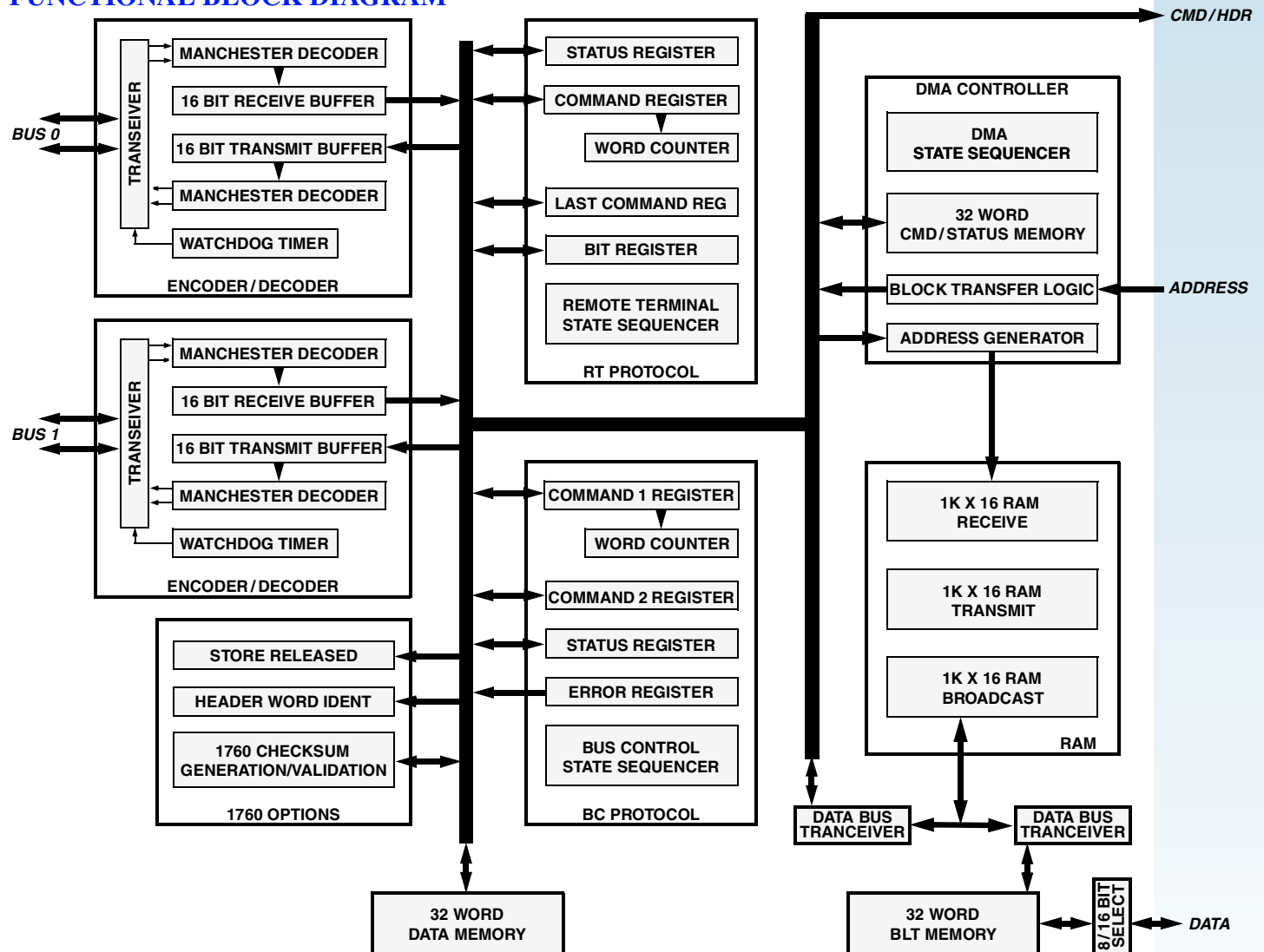
May 31, 2005



FEATURES

- ❑ Complete RT & BC Protocol
- ❑ Meets MIL-STD-1553 A/B & MIL-STD-1760 A/B
- ❑ 8 or 16 bit VME/MULTIBUS Interface
- ❑ 3K RAM
- ❑ Dual Transceivers (1553 / 1760 or McAir)
- ❑ +5V - Only Power Supply
- ❑ Low Power (0.15 Watts per Channel)
- ❑ Only Validated Messages Written to RAM
- ❑ Self Test
- ❑ Write/Readable Status & Bit Registers
- ❑ Block Transfer Logic Guarantees Data Consistency
- ❑ Optional Data Wrap Around
- ❑ Any Message may be Illegalized
- ❑ Reduced Response Time Option (inh MC1F, RT & BC)
- ❑ Optional 1760 checksum (RT & BC)
- ❑ 1760 Header word identification
- ❑ Store Released Signal
- ❑ Latched or Hard Wired RT Address
- ❑ Comprehensive BC Error Checking
- ❑ MIL-PRF-38534 Compliant Circuits Available
- ❑ Designed for Commercial, Industrial and Aerospace Applications
- ❑ Aeroflex is a Class H & K MIL-PRF-38534 Manufacturer

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

CT2577 provides the complete protocol for both Remote Terminal and Bus Controller, supporting all types of message transfers including all 15 mode codes, with comprehensive error checking. Error handling of data is not required by the subsystem.

The low power transceivers are capable of providing the output voltage required by MIL-STD-1760 and are powered by a +5V supply.

If sinusoidal (McAir) transceivers are required then the part number becomes CT2579 This is the only difference between CT2577 and CT2579

The user interface is pin selectable between 8 and 16 bit for both VME and MULTIBUS. Addresses are referred to in hexadecimal format and five bit address fields for simplicity in correlating to the MIL-STD-1553 commands.

The device contains 3K words of main memory (1K receive, 1K transmit, and 1K broadcast receive).

A FIFO type memory is also provided for storing up to 32 command words (RT) or 32 status responses (BC). Access to this memory is achieved by reading from location 0 00 00. Discrete signals are provided to indicate the memory status (i.e. full or empty). To reduce the processor intervention, the command / status memory will only store commands that have associated data.

A 32 word data buffer memory is used to store messages until validation is complete. Only validated messages are written to the main memory in a single burst. Data to be transmitted is transferred from the main RAM to this buffer memory in a single burst.

An optional 32 word BTL memory buffers the main memory to the subsystem. This memory ensures data consistency by "bursting" a message from the BTL memory to the main memory (write) or from main memory to BTL memory (read) uninterrupted after which the subsystem has access to this memory at its leisure. This memory is not used for mode commands as there is a maximum of only one associated data word and data inconsistency cannot occur. The BTL memory may be disabled by hardware or software.

Arbitration between the 1553 data bus and the processor bus is fully automatic. When the main memory is required to be accessed by the 1553 data bus, any current subsystem access to the main RAM is completed first, thus ensuring no data is lost or corrupted. The time the main memory is accessed by the 1553 data bus equates to 8.5 μ S for command or status words, plus 1 μ S (transmit) or 500 nS (receive) for each data word.

The device has an optional RT wrap around capability. When WRAPEN is active, data received at subaddress 1E (30) remains stored in the data buffer memory (i.e. not transferred to main memory). If followed by a transmit from subaddress 1E the same data will be transmitted.

A self test feature can be enabled by the subsystem in software. This function will initially set the device to be a Bus Controller and transmit a message.

This message is received by the Remote Terminal via the transceivers (online) or bypass the transceivers (offline). The data and command transmitted by the Bus Controller can be read back from the Remote Terminal by the subsystem.

There is an option within the device to reduce the response time in order to conform to other standards such as 1553A and McAir. In this mode subaddress 1F is allocated a normal subaddress for both Remote Terminal and Bus Controller with subaddress 00 being the only subaddress reserved for mode commands.

Any message may be illegalised by applying an active low on the NME discrete status input. The Remote Terminal will respond with the Message Error bit set in the status and not use the information received.

Configuration as a Remote Terminal and Bus Controller is achieved by writing to address 1 00 00 and 1 00 01 respectively. The device defaults to Remote Terminal on power up reset. A discrete signal BCNRT is provided to indicate the device mode. The option is available for the Remote Terminal to switch to Bus Control via the mode code Dynamic Bus Control.

In the Bus Control mode all commands transferred to the device are error checked and only valid legal commands are allowed to be transmitted onto the 1553 data bus, any errors are reported back to the host. Messages received on the 1553 data bus destined for the host will only be stored in the main memory once they have been completely validated.

A hardware implementation of the 1760 checksum algorithm within the device may be enabled for both Remote Terminal and Bus Controller via signal NENCHK. When transmitting, the checksum word is inserted in the last word position, and when receiving, a valid checksum word will generate the signal NVALCHK as well as an open drain output (STATUS). The STATUS output may be hard wired to any of the discrete status inputs (e.g. Service Request), if it is also hard wired to the input NILLCMD the device will respond to a failed checksum with the selected status bit set and not use the data (i.e. not write to main memory).

In addition to the signal NVCR (valid command word received) which may be used to illegalise commands, a signal NHDR (header word received) is available to the subsystem for verification of the 1760 message header.

The RT address lines may be continuously monitored or latched on RESET as required by 1760. If all six RT address lines go open circuit the store released signal (STREL) will go high.

A signal is provided to monitor the internal watchdog timers for test purposes. A set of pins are available to connect additional external watchdog timers if so desired.

As well as being able to set the Remote Terminal status bits discretely they may be written to via the VME/MULTIBUS interface. These status bits as well as the status of the Block Transfer Logic and Self Test function may be read back from the device.

A software write / readable BIT register is available.

SIGNAL DESCRIPTIONS

1553 / 1760 DATA BUS

DATABUS 0 (Bidirectional)

Signal is connected to the positive side of the external data bus transformers for bus 0.

NDATABUS 0 (Bidirectional)

Signal is connected to the negative side of the external data bus transformers for bus 0.

DATABUS 1 (Bidirectional)

Signal is connected to the positive side of the external data bus transformers for bus 1.

NDATABUS 1 (Bidirectional)

Signal is connected to the negative side of the external data bus transformers for bus 1.

WATCHDOG (Output)

Signal monitors internal watchdog timer, will go high at the start of a transmission and remain high for 800 μ S. If a new command is received before the signal times out it will be reset.

NTXINH 0 (Input with pull up resistor)

Input to inhibit transmissions onto channel 0 of the 1553 data bus. External watchdog timer would be connected to this input. May be left open circuit if not used.

"0" = Inhibit
"1" = Enable

NTXINH 1 (Input with pull up resistor)

Input to inhibit transmissions onto channel 1 of the 1553 data bus. External watchdog timer would be connected to this input. May be left open circuit if not used.

"0" = Inhibit
"1" = Enable

SELEN 0 (Output)

Output high indicates that the last command received by the Remote Terminal was on channel 0 of the 1553 data bus or channel 0 has been selected by the Bus Controller. Used to select watchdog timer channel.

SELEN 1 (Output)

Output high indicates that the last command received by the Remote Terminal was on channel 1 of the 1553 data bus or channel 1 has been selected by the Bus Controller. Used to select watchdog timer channel.

INITWD (Output)

Output indicates that a transmission onto the selected 1553 data bus is about to commence. Used to initiate an external watchdog timer. The signal is a 250 nS active low pulse.

HARD WIRED

ADDR A-E (Inputs with pull up resistor)

Remote Terminal address inputs for the unit. ADDR A is the least significant bit and ADDR E is the most significant bit.

ADDR P (Input with pull up resistor)

Parity bit for the Remote Terminal address inputs. ADDR P must be set to ODD parity.

LA (Input with pull up resistor)

Input enables the Latched Address option. Normally the Remote Terminal address inputs are constantly monitored and compared with the incoming command word. When enabled the Remote Terminal address inputs are internally latched every time the unit is reset. The latched address information is then compared to the incoming command word. This latched Remote Terminal address function complies with the requirements of 1760. If left open circuit the device will default to the latched address mode,

"0" = RT address inputs are NOT latched
"1" = RT address inputs ARE latched

VME (Input with pull up resistor)

Select VME or MULTIBUS subsystem interface. If left open circuit the device will default to VME mode.

"0" = Multibus mode
"1" = VME mode

NBIT16 (Input with pull down resistor)

Select 8 or 16 bit subsystem data interface. In 8 bit mode only the lower 8 bits of the data bus (DATA 0-7) are used for all data transfers. If left open circuit the device will default to 16 bit mode.

"0" = 16 bit mode
"1" = 8 bit mode

WRAPEN (Input with pull down resistor)

Select Remote Terminal wrap around to subaddress 1E. For this test to work correctly the unit must be in RT mode. The Bus Controller sends data to subaddress 1E. The data received is stored in the "transmit" area of the main RAM and the Command word is stored in the Command / Status memory as described in BC to RT transfer. The device will respond with status. The Bus Controller will then send a transmit command to subaddress 1E and the data contained in the "transmit" area of the main RAM will be transmitted following the status and the Command word which is stored in the Command / Status memory as described in RT to BC transfer.

"0" = Normal mode
"1" = Wrap Around mode

MCAIR (Input with pull down resistor)

This signal sets the unit to respond with a status word within 4 μ S (dead bus time) while in Remote Terminal mode. Subaddress 1F is also enabled to be a valid subaddress for data. Normally subaddress 00 and 1F are reserved for mode codes.

"1" = 4 μ S dead bus response time, subaddress 1F used for data.
"0" = 12 μ S response time, subaddress 1F used for mode codes.

NENBTL (Input with pull up resistor)

Signal to enable the Block Transfer Logic. When active a 32 word RAM is inserted as a buffer between the main RAM and the subsystem. This memory guarantees data consistency by bursting a message from the BTL memory to the main memory (write) or from main memory to BTL memory (read) uninterrupted. The Block Transfer Logic may be selectively disabled in software giving the subsystem direct access to the main RAM.

"0" = Enable Block Transfer Logic
"1" = Disable Block Transfer Logic and software selection.

C16MHZ (Input with pull up resistor)

Free running 16 MHz clock input.

VME/MULTIBUS INTERFACE

ADIN 0-11 (Inputs with pull up resistor)

12 bit address input to the unit specifying what location the user will be accessing in the RAM / registers. These address inputs are inverted when the Multibus interface is selected.

DATA 0-15 (Bidirectional IO)

16 bit bidirectional data highway access to internal RAM and registers. When in 8 bit mode only DATA 0-7 are used. Data inputs / outputs are inverted when the Multibus interface is selected.

UB (Input with pull up resistor)

Upper byte: When the unit is in 8 bit mode this signal is used as the LSB of the address lines. In 16 bit mode the signal is not used and the LSB of the address lines is ADIN 0.

NCARDEN (Input with pull up resistor)

Signal to indicate the processor is addressing this unit. The user can use this signal tied to an address decoder to enable the unit for a read/write operation.

"0" = Enable unit for I/O operations.

NRD (Input with pull up resistor)

VME Mode: Data Strobe for a data transfer.

"0" = Write / Read data to/from the subsystem.

"1" = Tristate the Data 0-15 bus.

Multibus Mode: Read strobe for a data transfer.

"0" = Read data from the unit to the subsystem.

"1" = Tristate the Data 0-15 bus.

NWR (Input with pull up resistor)

VME Mode: Write / Read direction flag for NRD data strobe.

"0" = Write data from subsystem to device.

"1" = Read data from device to subsystem.

Multibus Mode: Write strobe for a data transfer.

"0" = Write data from subsystem to device.

"1" = Tristate the Data 0-15 bus.

NACK (Open drain output)

After a write / read cycle has begun, this signal indicates that the write / read operation to the unit has been acknowledged and that access has been granted. Read data is available and write data is complete. The user can complete the write / read cycle.

"0" = Cycle is acknowledged, access granted.

"1" = No acknowledge, wait.

NEMPTY (Output)

Empty flag for the Command / Status FIFO memory which can store up to 32 command words (RT) or 32 status words (BC). In RT mode the memory will store all command words that have accessed the main RAM. This includes all standard commands to receive and transmit data from the main RAM and mode codes with data that require subsystem involvement ie. Synchronize With Data and Transmit Vector Word. In BC mode all status responses are stored in this memory. Access to this memory is gained by reading from address 0 00 00.

"0" = Memory is empty, no words to read.

"1" = Memory is not empty, has words to read.

NFULL (Output)

Full flag for the Command / Status FIFO memory. When the signal goes low the memory is full and will not store any more data.

T0-T15 (Output)

16 bit output highway monitors the internal data bus of the unit. This allows the user to have access to the 1553 data bus traffic in real time. The user can utilise this bus for message illegalization and read words such as Command, Data, Synchronize and Header word (1760 requirement).

DISCRETE RT STATUS INPUTS

The following signals are inputs to set the appropriate bits in the Remote Terminals status word. All inputs are sampled after NVCR except non mode code receive commands in which case they are sampled after the last data word has been received. All status inputs are active low.

NME (Input with pull up resistor)

Message Error, illegalises message. Command will not be stored in Command / Status memory and no transfers to / from main RAM will take place. No data will be transmitted following the status.

NBUSY (Input with pull up resistor)

Subsystem Busy. No data will be transferred to / from main RAM and no data will be transmitted following status.

NTF (Input with pull up resistor)

Terminal Flag.

NSR (Input with pull up resistor)

Service Request.

NSSFLAG (Input with pull up resistor)

Subsystem Flag.

NDBCA (Input with pull up resistor)

Dynamic Bus Control Acceptance.

RT DISCRETE SIGNALS

NRES (Bidirectional IO with pull up resistor)

Bidirectional reset pin. Interface to this pin should be in the form of an open collector pull down driver. The unit will be reset when a low level input is asserted on power up. The pin is bidirectional in that the unit will drive the signal out low after the status response of the mode code Reset Remote Terminal. Upon reset the unit will initialise to RT mode and will be able to respond immediately after the rising edge of NRES.

NILLCMD (Input with pull up resistor)

Input to illegalise a command to the Remote Terminal with a clear status response. The signal is sampled after NVCR except non mode code receive commands in which case it is sampled after the last data word has been received. A low on this input will illegalise the message, Command will not be stored in the Command / Status memory and no transfers to / from main RAM will take place. The device will respond with a clear status unless a bit has been specifically set. No data will be transmitted following status.

INHMC (Input with pull down resistor)

Inhibit Mode Code: subaddress 00 and 1F are treated as normal non mode code transmit or receive commands. For use in RT mode only. May be left open circuit for normal operation.

"0" = Normal operation.

"1" = Inhibit all mode codes.

NVCR (Output)

Early indication that the Remote Terminal has received a command and the command word is available on T0-T15. This can be used for message illegalization.

NDATA (Output)

Access to valid data word in real time before being written to RAM. Data word available on T0-T15 during active low signal.

NCMDSTRB (Output)

This signal indicates that a completely validated message has been received for standard subaddress data activity. Mode commands with or without data will not generate this signal. The NCMDSTRB signal is 8.5 μ S long and is an indication that a DMA burst will initiate at the end of NCMDSTRB to transfer words between the 32 word data memory and the internal main RAM. All subsystem read / writes to the main RAM that have been acknowledged (NACK = "0") before NCMDSTRB has begun must now be completed within 8.5 μ S. All subsystem read / write requests to the main RAM initiated after NCMDSTRB has begun will be held off (no acknowledge) until the DMA cycle has been completed. The length of the DMA cycle is dependant on the number of words to DMA into RAM. Access to the 32 word BTL memory is still possible during the DMA cycle by the subsystem. However, transfers between the BTL memory and the main RAM will be locked out.

BCST (Output)

Output high indicates command received was a broadcast. Signal will remain high until next command is received.

MCDET (Output)

Output high indicates command received was a mode command. Signal will remain high until next command is received.

NSYNC (Output)

Signal to subsystem indicating receipt of a Synchronize mode commands. If the mode code has an associated data word, it will be available on T0-T15 at this time. If there is no associated data word, T0-T15 will be zero.

BC DISCRETE SIGNALS

NNEWBUS (Input with pull up resistor)

A Bus Control sequence may not normally be initiated until the current sequence is completed, indicated by signal EOT. However, the Bus Control sequence may be terminated and restarted if NNEWBUS is active low along with write to address 0 00 00. This feature would only be used in bus switching.

EOT (Output)

Valid transfer on 1553 data bus selected has been completed.

"0" = Transfer in progress.

"1" = Transfer complete.

NDBC (Output)

Active low indicates that the command received by the Remote Terminal was mode code Dynamic Bus Control. Signal will remain low until next command is received.

BCNRT (Output)

Indicates what mode the unit is in.

"0" = Remote Terminal.

"1" = Bus Controller.

ERROR (Output)

Indication that an error has occurred either in the information transferred to the unit from the subsystem or in the transfers on the 1553 data bus. Nature of error is available by reading from register location 0 00 12.

NSTSTRB (Output)

This signal goes low for 8.5 μ S to indicate a valid transfer has been completed on the 1553 data bus and the received Status word is now available on the T0-T15 highway. The Status word is also stored in the Command / Status memory at this time. Once the signal goes high data received by the Bus Controller (RT to BC transfer) will be transferred to the main RAM from the 32 word data buffer memory. Note: Data transferred in RT to RT transfers is not stored in the Bus Controller's main RAM.

NINHST (Input with pull up resistor)

May be used to illegalise a message just received. Signal can be tied to STATUS for illegalization due to 1760 checksum failures. A low will prevent any data received being transferred to the main RAM, and the Status word will not be stored in the Command / Status memory.

1760 SIGNALS

NENCHK (Input with pull up resistor)

Enables / disables the internal hardware checksum generation and validation for both Remote Terminal and Bus Controller. When enabled, the circuitry will check all incoming data for correct checksum and generate the correct checksum word for an outgoing data transfer.

"0" = Enable checksum circuitry.

"1" = Disable checksum circuitry.

STATUS (Open drain output)

Open drain output will toggle high or low on each incoming data word from the 1553 data bus provided NENCHK is enabled. When the last data word is received the STATUS line is sampled by the protocol circuitry to determine if the checksum for the message is valid. At the end of the message, if STATUS is low then the checksum is not valid. This STATUS signal can be wired to several different pins to customise the units response to a checksum failure. STATUS can be wired to signals such as NILLCMD and NSR which would cause the message to be illegalised and set Service Request bit in the Status.

NVALCHK (Output)

Latched version of the STATUS signal. NVALCHK is latched on the falling edge of NCMDSTRB (RT) or NSTSTRB (BC) and will remain stable until the next NCMDSTRB or NSTSTRB.

"0" = Checksum word was not valid.

"1" = Checksum word was valid.

NHDR (Output)

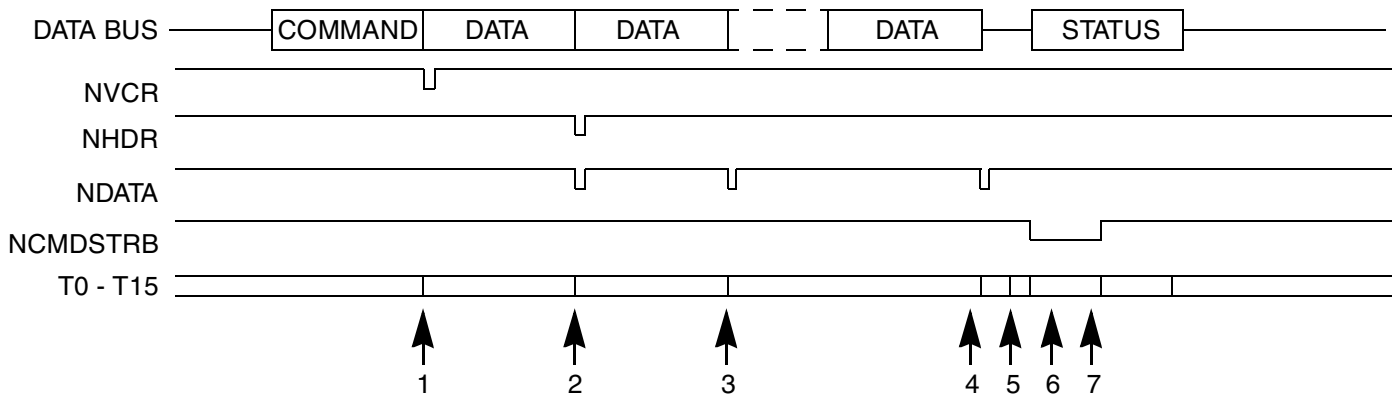
In Mil-Std-1760, the first data word of a message is defined as a Header word. The NHDR signal indicates the presence of the Header word on the T0-T15 highway as it is received. The user can also read the Header word from RAM.

STREL (Output)

When the store is released from the aircraft all the Remote Terminal address inputs go high causing signal STREL to go high.

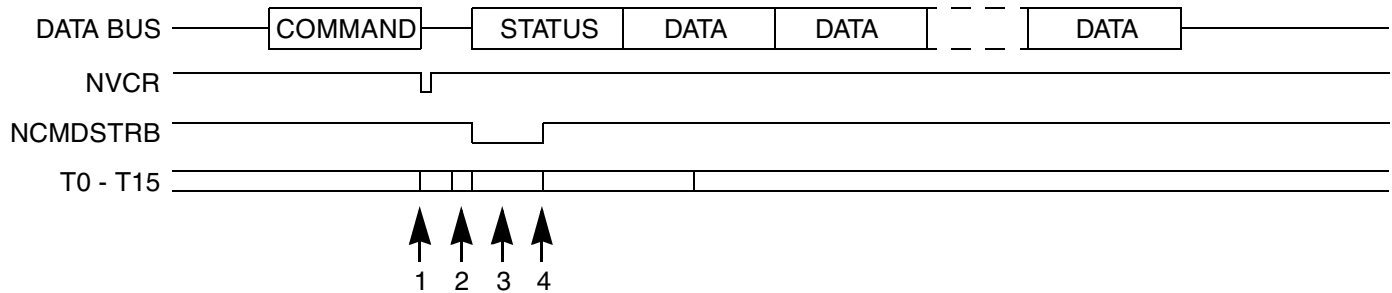
MESSAGE FORMATS (RT)

BC TO RT TRANSFER



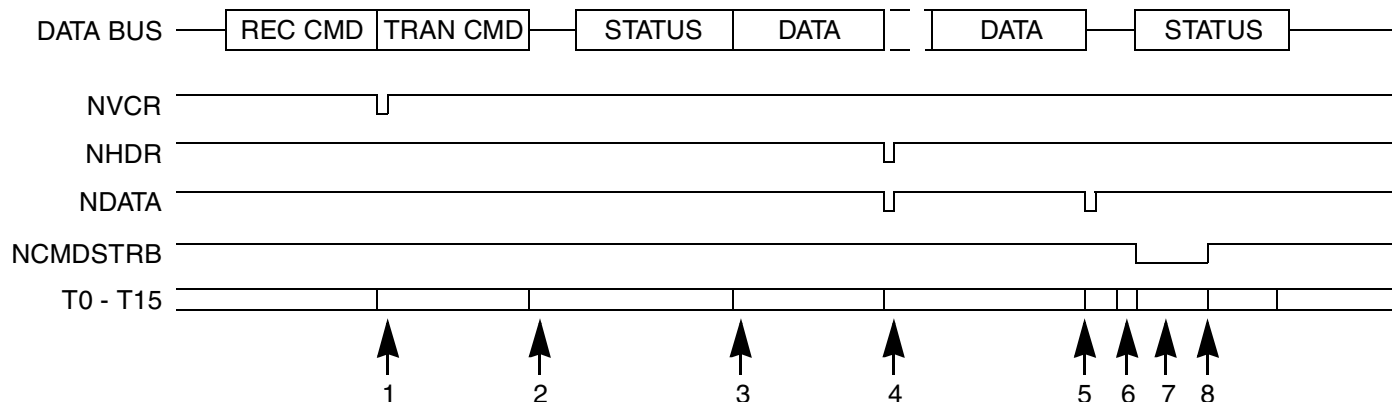
1. Valid command word received, contents available on T0-T15 for illegalization purposes.
2. First valid data word (1760 header word) received, contents available on T0-T15 and stored in 32 word data memory.
3. Second valid data word received, contents available on T0-T15 and stored in 32 word data memory.
4. Last valid data word received, contents available on T0-T15 and stored in 32 word data memory. Status bits must be valid within 250nS.
5. Status register contents transferred to transmit buffer.
6. NCMDSTRB indicates valid message received, command word available on T0-T15 and stored in the 32 word command memory.
7. Data words transferred from 32 word data memory to main memory at 500 nS per word.

RT TO BC TRANSFER



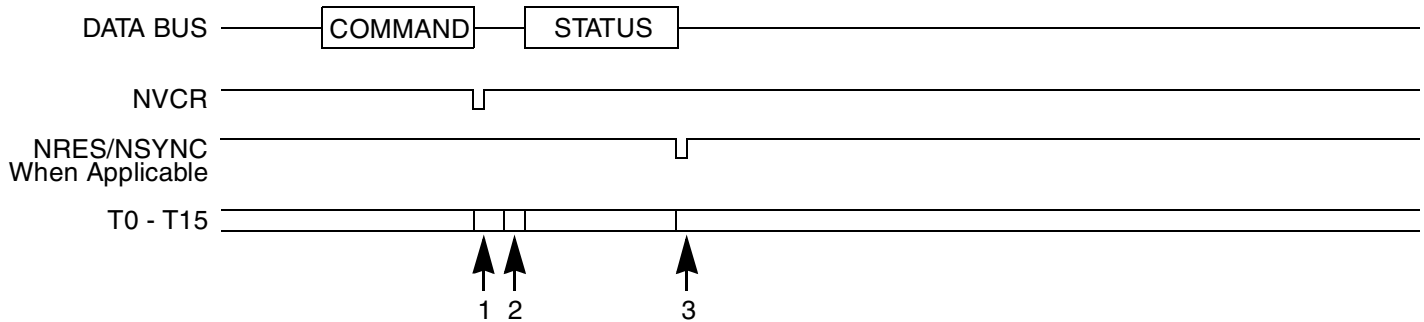
1. Valid command word received, contents available on T0-T15 for illegalization purposes. Status must be valid within 600 nS.
2. Status register contents transferred to transmit buffer.
3. NCMDSTRB indicates valid message received, command word available on T0-T15 and stored in the 32 word command memory.
4. Data words transferred from main memory to 32 word data memory at 1 μ S per word.

RT TO RT TRANSFER (RECEIVING TERMINAL)



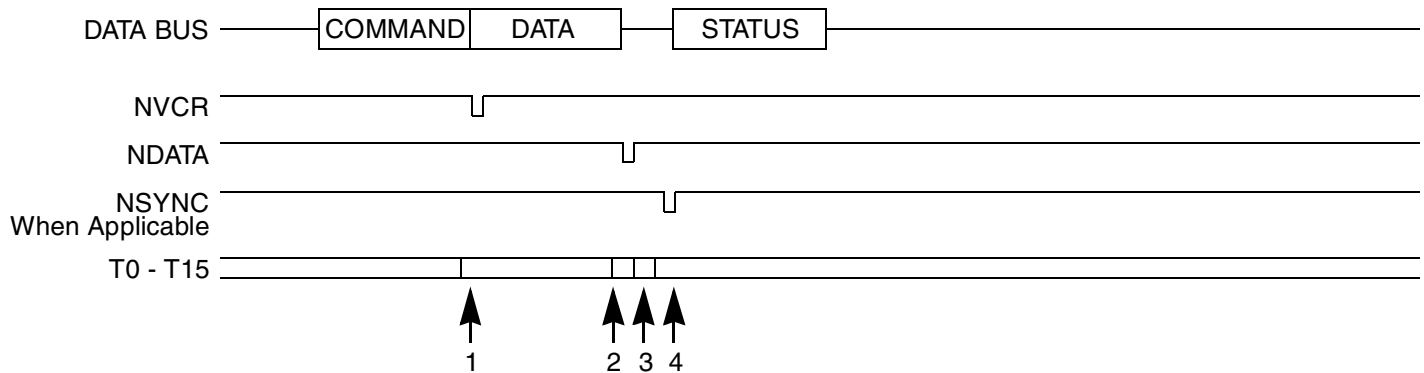
1. Valid receive command word received, contents available on T0-T15 for illegalization purposes.
2. Valid transmit command word received, contents available on T0-T15.
3. Status response of transmitting terminal received.
4. First valid data word (1760 header word) received, contents available on T0-T15 and stored in 32 word data memory.
5. Last valid data word received, contents available on T0-T15 and stored in 32 word data memory. Status bits must be valid within 250nS.
6. Status register contents transferred to transmit buffer.
7. NCMDSTRB indicates valid message received, command word available on T0-T15 and stored in the 32 word command memory.
8. Data words transferred from 32 word data memory to main memory at 500 nS per word.

MODE CODES WITHOUT DATA



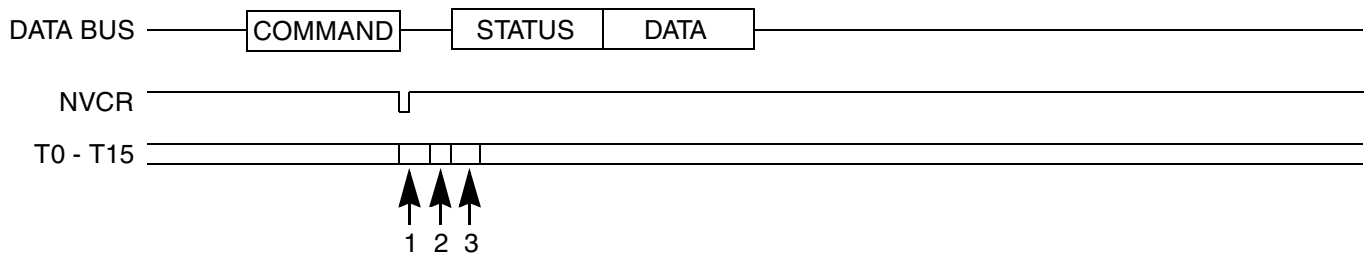
1. Valid command word received, contents available on T0-T15 for illegalization purposes. Status must be valid within 600 nS.
2. Status register contents transferred to transmit buffer.
3. Synchronize mode command, T0-T15 = 0.

MODE CODES WITH DATA RECEIVE



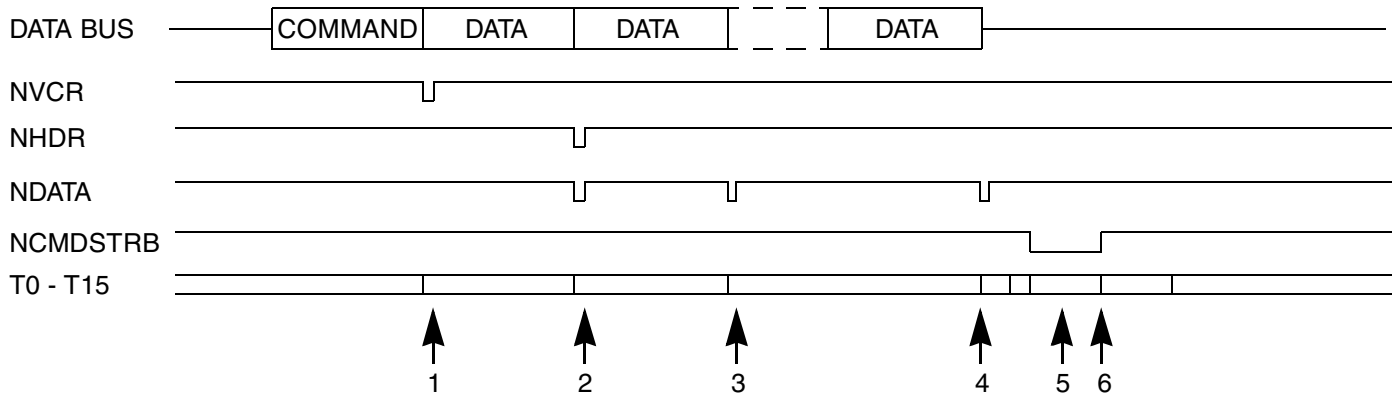
1. Valid command word received, contents available on T0-T15 for illegalization purposes. Status must be valid within 600 nS.
2. Valid data word received, contents available on T0-T15. Synchronize data word stored in 32 word data memory.
3. Status register contents transferred to transmit buffer after message validation.
4. Synchronize data word (when applicable) transferred from 32 word data memory to main memory and available on T0-T15.

MODE CODES WITH DATA TRANSMIT



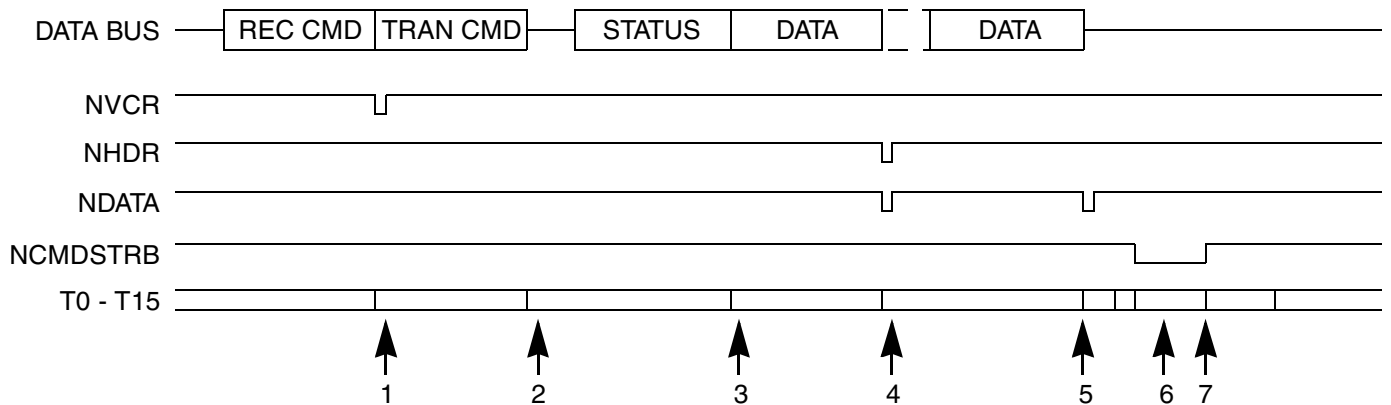
1. Valid command word received, contents available on T0-T15 for illegalization purposes. Status must be valid within 600 nS.
2. Status register contents transferred to transmit buffer after message validation.
3. Vector word or BIT word (when applicable) transferred from main memory to transmit buffer.

BC TO RT TRANSFER BROADCAST



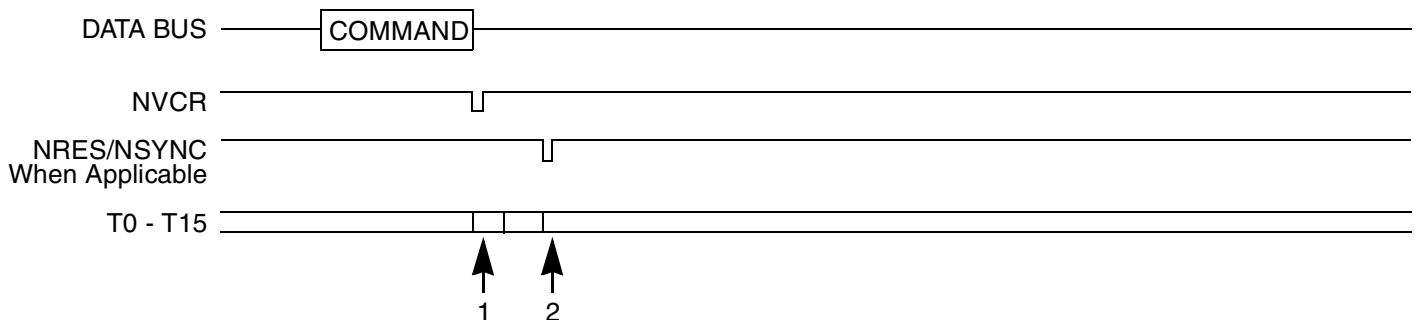
1. Valid command word received, contents available on T0-T15 for illegalization purposes.
2. First valid data word (1760 header word) received, contents available on T0-T15 and stored in 32 word data memory.
3. Second valid data word received, contents available on T0-T15 and stored in 32 word data memory.
4. Last valid data word received, contents available on T0-T15 and stored in 32 word data memory. Status bits must be valid within 250nS.
5. NCMDSTRB indicates valid message received, command word available on T0-T15 and stored in the 32 word command memory.
6. Data words transferred from 32 word data memory to main memory at 500 nS per word.

RT TO RT TRANSFER BROADCAST (RECEIVING TERMINAL)



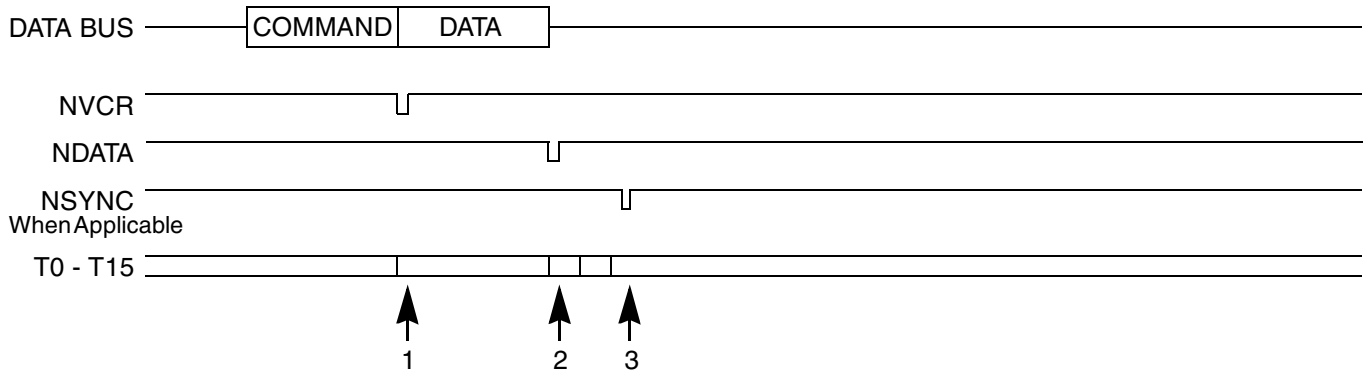
1. Valid receive command word received, contents available on T0-T15 for illegalization purposes.
2. Valid transmit command word received, contents available on T0-T15.
3. Status response of transmitting terminal received.
4. First valid data word (1760 header word) received, contents available on T0-T15 and stored in 32 word data memory.
5. Last valid data word received, contents available on T0-T15 and stored in 32 word data memory. Status bits must be valid within 250nS.
6. NCMDSTRB indicates valid message received, command word available on T0-T15 and stored in the 32 word command memory.
7. Data words transferred from 32 word data memory to main memory at 500 nS per word.

MODE CODES WITHOUT DATA BROADCAST



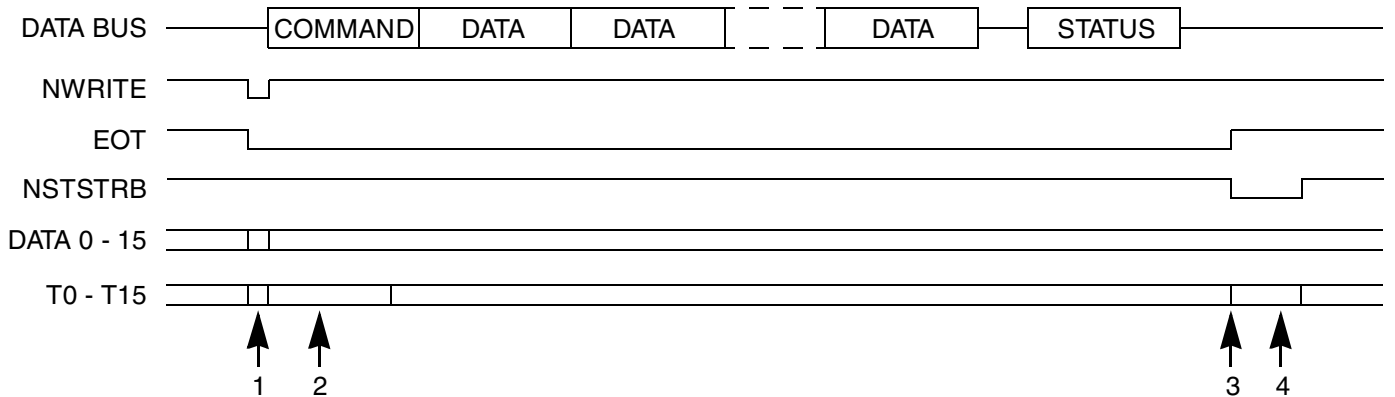
1. Valid command word received, contents available on T0-T15 for illegalization purposes. Status must be valid within 600 nS.
2. Synchronize mode command, T0-T15 = 0.

MODE CODES WITH DATA RECEIVE BROADCAST



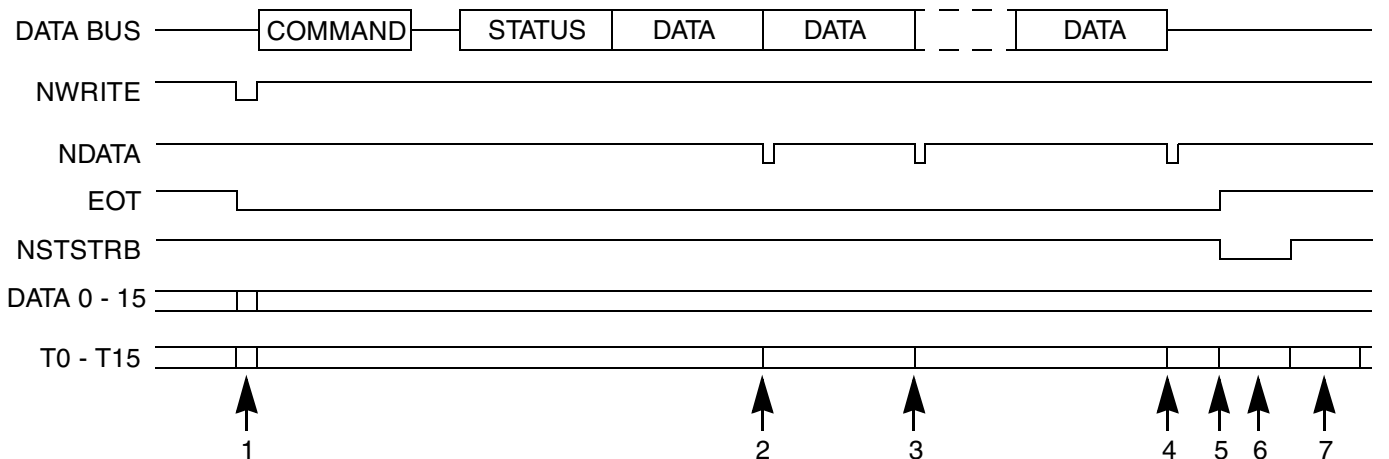
1. Valid command word received, contents available on T0-T15 for illegalization purposes. Status must be valid within 600 nS.
2. Valid data word received, contents available on T0-T15. Synchronize data word stored in 32 word data memory.
3. Synchronize data word (when applicable) transferred from 32 word data memory to main memory and available on T0-T15.

MESSAGE FORMATS (BC) BC TO RT TRANSFER



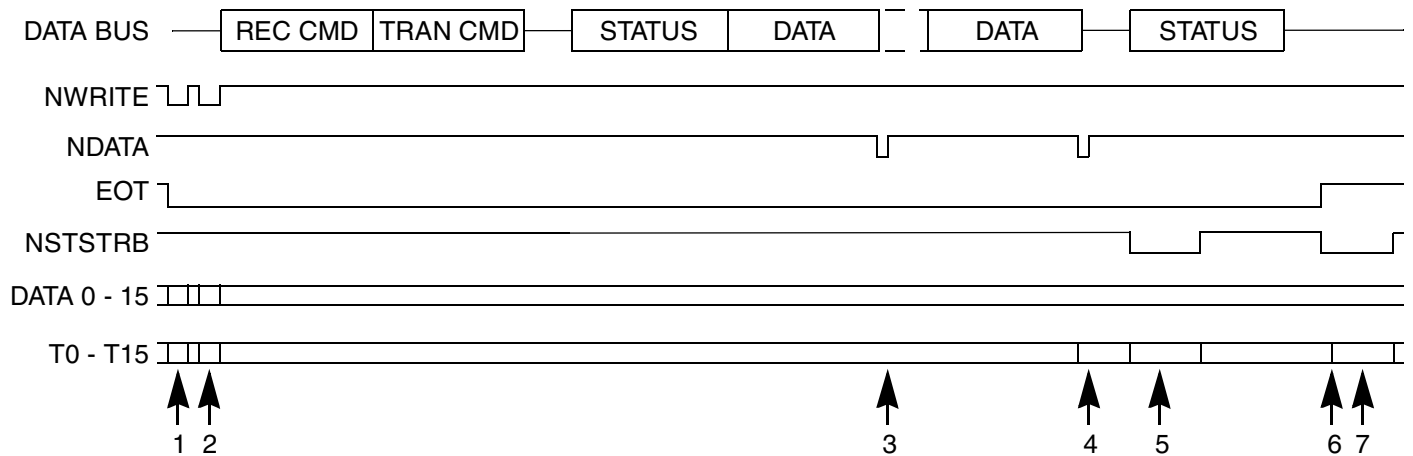
1. Write command to address 0 00 00.
2. Data words transferred from main memory to 32 word data memory at 1 μ S per word.
3. End of data bus transfers.
4. NSTSTRB indicates valid message transferred, status word available on T0-T15 and stored in the 32 word status memory.

RT TO BC TRANSFER



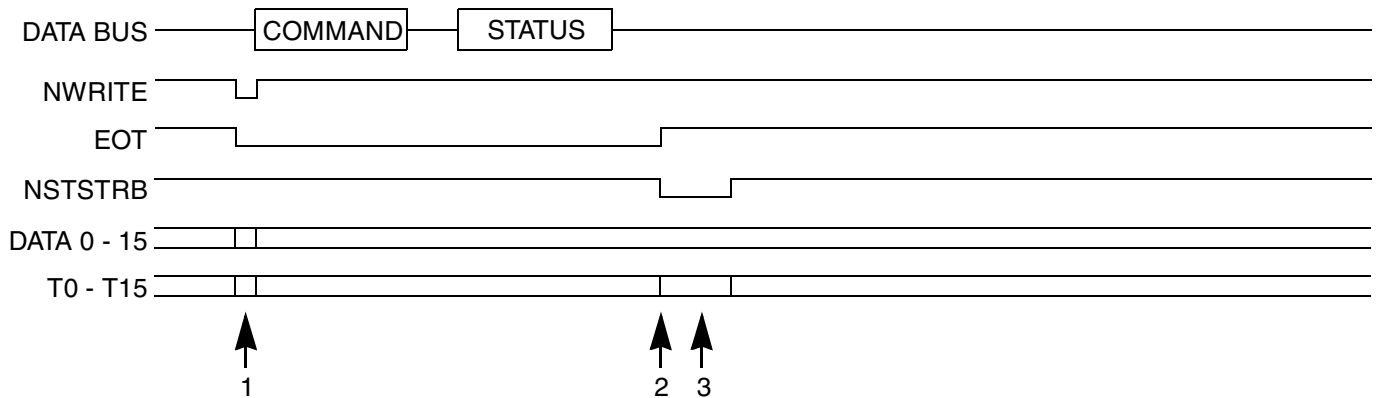
1. Write command to address 0 00 00
2. First data word received, contents available on T0-T15 and stored in 32 word data memory.
3. Second data word received, contents available on T0-T15 and stored in 32 word data memory.
4. Last data word received, contents available on T0-T15 and stored in 32 word data memory.
5. End of data bus transfers.
6. NSTSTRB indicates valid message transferred, status word available on T0-T15 and stored in the 32 word status memory.
7. Data words transferred from 32 word data memory to main memory at 1 μ S per word.

RT TO RT TRANSFER



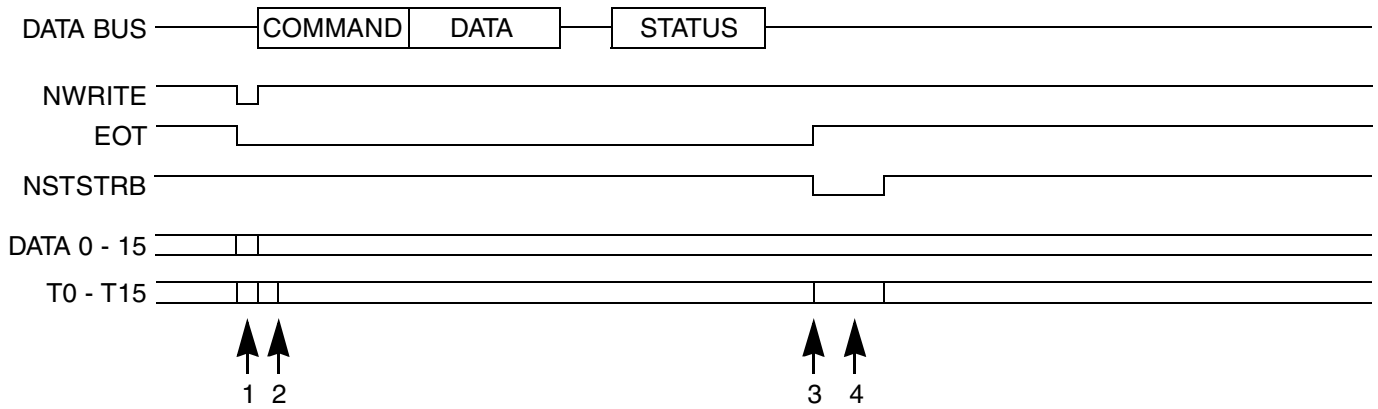
1. Write receive command to address 0 00 01.
2. Write transmit command to address 0 00 00.
3. First data word received, contents available on T0-T15.
4. Second data word received, contents available on T0-T15.
5. NSTSTRB indicates valid message transferred by the transmitting terminal, its status word is available on T0-T15 and stored in the 32 word status memory.
6. End of data bus transfers.
7. NSTSTRB indicates valid message transferred to the receiving terminal, its status word is available on T0-T15 and stored in the 32 word status memory.

MODE CODES WITHOUT DATA



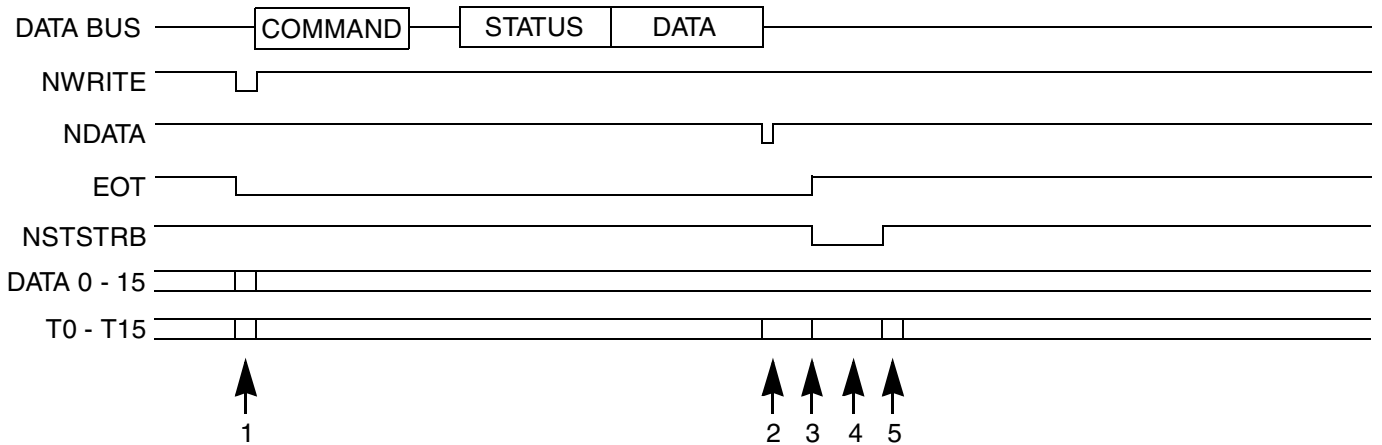
1. Write command to address 0 00 00.
2. End of data bus transfers.
3. NSTSTRB indicates valid message transferred, status word available on T0-T15 and stored in the 32 word status memory.

MODE CODES WITH DATA RECEIVE



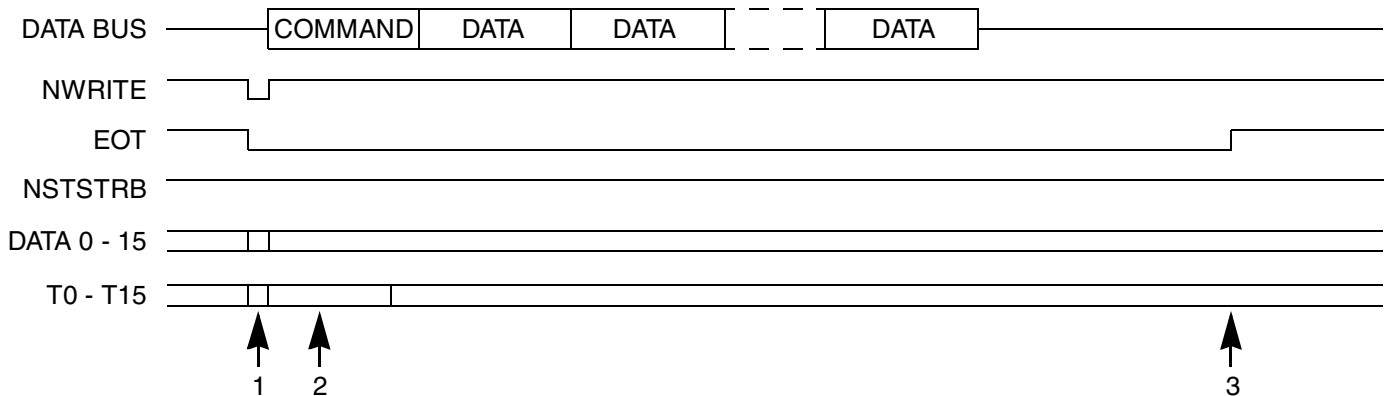
1. Write command to address 0 00 00.
2. Data word transferred from main memory to 32 word data memory.
3. End of data bus transfers.
4. NSTSTRB indicates valid message transferred, status word available on T0-T15 and stored in the 32 word status memory.

MODE CODES WITH DATA TRANSMIT



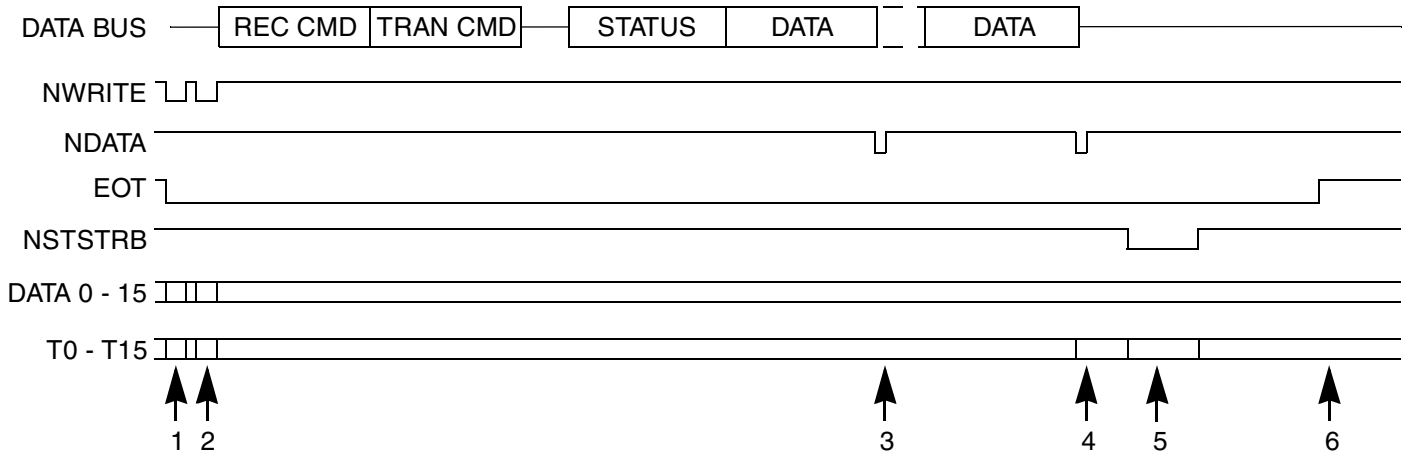
1. Write command to address 0 00 00
2. Data word received, contents available on T0-T15 and stored in 32 word data memory.
3. End of data bus transfers.
4. NSTSTRB indicates valid message transferred, status word available on T0-T15 and stored in the 32 word status memory.
5. Data word transferred from 32 word data memory to main memory.

BC TO RT TRANSFER BROADCAST



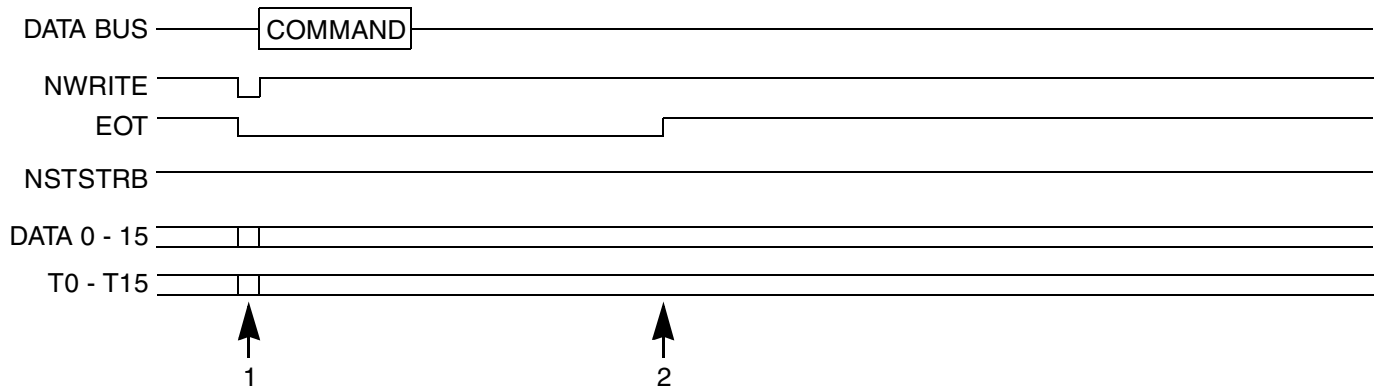
1. Write command to address 0 00 00.
2. Data words transferred from main memory to 32 word data memory at 1 μ S per word.
3. End of data bus transfers.

RT TO RT TRANSFER BROADCAST



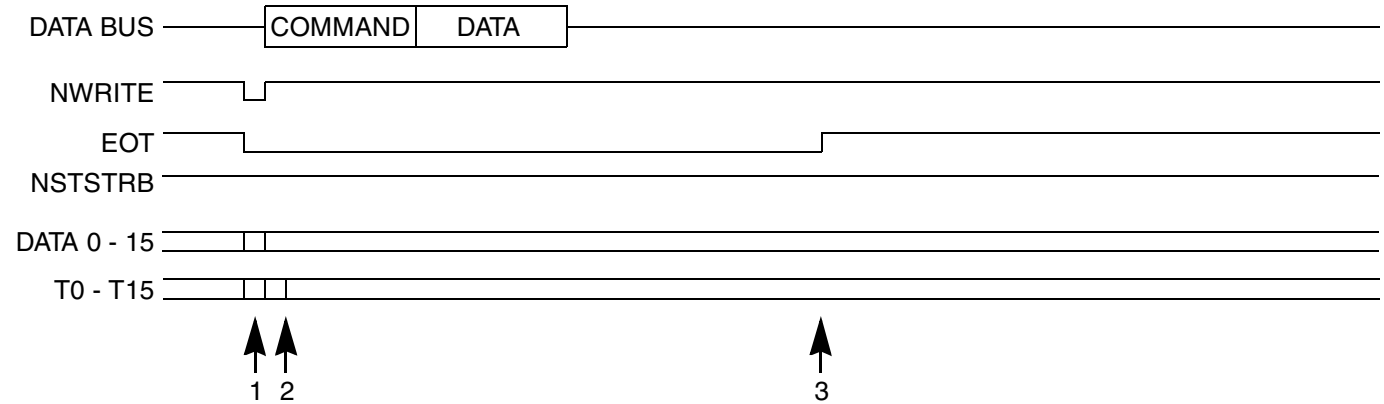
1. Write receive command to address 0 00 01.
2. Write transmit command to address 0 00 00.
3. First data word received, contents available on T0-T15.
4. Second data word received, contents available on T0-T15.
5. NSTSTRB indicates valid message transferred by the transmitting terminal, its status word is available on T0-T15 and stored in the 32 word status memory.
6. End of data bus transfers.

MODE CODES WITHOUT DATA BROADCAST



1. Write command to address 0 00 00.
2. End of data bus transfers.

MODE CODES WITH DATA RECEIVE BROADCAST



1. Write command to address 0 00 00.
2. Data word transferred from main memory to 32 word data memory.
3. End of data bus transfers.

REMOTE TERMINAL OPERATION

The unit will default to Remote Terminal mode on application of a “Power Up” reset.

TRANSMIT COMMAND

Upon receipt of a validated transmit command the device performs the following functions:

- a) Respond with status.
- b) Load command word into address pointer.
- c) Write command word into Command / Status memory. If the Busy bit is set the sequence is terminated.
- d) Switch the RAM to 1553 mode.
- e) Transfer data words from main RAM to data buffer memory, transmit data and decrement address until zero.
- f) Switch RAM back to processor access.

RECEIVE COMMAND

Upon receipt of a fully validated message the device performs the following functions:

- a) Respond with status (not broadcast).
- b) Load command word into address pointer.
- c) Write command word into Command / Status memory. If the Busy bit is set the sequence is terminated.
- d) Switch the RAM to 1553 mode.
- e) Write data words to RAM and decrement address until zero.
- f) Switch RAM back to processor access.

MODE CODES

Mode codes requiring non subsystem intervention are handled automatically by the device. Hence none of these command words are entered into the Command / Status memory.

These mode codes are:

Synchronize Without Data Word
Transmit Status
Initiate Self Test (see detail)
Transmitter Shutdown
Override Transmitter Shutdown
Inhibit Terminal Flag
Override Inhibit Terminal Flag
Reset Remote Terminal
Transmit Last Command
Selected Transmitter Shutdown
Override Selected Transmitter Shutdown

MODE CODES REQUIRING SUBSYSTEM ACCESS

Synchronize With Data Word

Upon receipt of a validated message the device performs the following functions:

- a) Respond with status (not broadcast).
- b) Write command to the Command / Status memory.
- c) Switch the RAM to 1553 mode.
- d) The associated data word is written into RAM location 0 00 11 or 0 1F 11.
- e) Switch the RAM back to processor access.

Transmit Vector Word

Upon receipt of a validated message the device performs the following functions:

- a) Respond with status.
- b) Write the command to the Command / Status memory.
- c) Switch the RAM to 1553 mode.
- d) Transfer the data word from RAM location 1 00 10 or 1 1F 10 and transmit.
- e) Switch the RAM back to processor access.

Transmit Bit Word

Upon receipt of a validated message the device performs the following functions:

- a) Respond with status.
- b) Command is not written to the Command / Status memory.
- c) Switch the RAM to 1553 mode.
- d) Transfer the data word from RAM location 1 00 13 or 1 1F 13 and transmit.
- e) Switch the RAM back to processor access.

Dynamic bus control

The device will respond with Status. If the Remote Terminal will accept dynamic bus control, RAM address 0 00 01 must be written to prior to receipt of the mode codes. The status word will then contain the Dynamic Bus Control Acceptance bit set. The output NDBC should be used by the background processor as either an interrupt or discrete signal. The status bit may alternatively be set discretely via input NDBCA. If the mode code is accepted the terminal must be switched to Bus Controller by writing to address 1 00 01.

RESERVED MODE CODES

These mode codes do not require subsystem intervention or illegalization. They will automatically be treated as illegal by the device. The unit will respond with Status with the Message Error bit set.

STATUS WORD BITS

There are four Status word bits that can be altered by the subsystem through write operations. These status bits may be set by writing to the following address locations:-

- | | | |
|-----------------------------------|---------|---------|
| a) Service Request | 0 00 08 | (Bit 3) |
| b) Subsystem Busy | 0 00 04 | (Bit 2) |
| c) Subsystem Flag | 0 00 02 | (Bit 1) |
| d) Dynamic Bus Control Acceptance | 0 00 01 | (Bit 0) |

The state of these bits are implemented in a four bit latch at address 0 00 0x. The input to the latches are the address line inputs. The data bus lines are not used at all.

Multiple Status bits may be set in a single write operation. For example to set Service Request and Subsystem Busy, address bits 2 and 3 should be set (ie. write to address 0 00 0C).

Writing to address 0 00 00 will reset status bits to zero. Alternatively status bits may be set discretely.

REMOTE TERMINAL DETAIL

COMMAND REGISTER

| | | | | | | | | | | | | | | | |
|------------|----|----|----|----|--------|--------------------------|---|---|---|---|--------------------------|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RT ADDRESS | | | | | T R | SUBSYSTEM ADDR / MODE | | | | | WORD COUNT / MODECODE | | | | |

The five most significant bits of the command register contain the Remote Terminal Address.

Bit 10 of the register is the Transmit / Receive bit. If it is set to '1' the device will perform the transmit sequence and it is set to '0' it will perform the receive sequence.

Bits 5 to 9 contain the Subsystem Address but two of these addresses are reserved and one programmable. 11111 (1F) or 00000 (00) indicate that the command is a mode code. The least significant five bits of the command register are used to decode the mode code and are not used as the word counter as a mode code may only have a maximum of one associated word.

111110 (1E) and WRAPEN sets the sequencer up to perform the wrap around function.

The least significant five bits of the command register contain the number of data words to be transmitted or received. 11111 is 31 words and 00000 is 32 words.

STATUS REGISTER

| | | | | | | | | | | | | | | | |
|------------|----|----|----|----|--------|----------|--------|-------|---|----------|----------|----------|----------|--------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RT ADDRESS | | | | | M E | IN ST | S R | RESVD | | BC ST | BU SY | SS FL | DB CA | T F | |

ME

Message Error: Set internally as a result of an error in the received message or set externally with a discrete pin to illegalise a message.

INST

Instrumentation: Set to zero.

SR

Service Request: Set with a discrete pin or by writing to address 0 00 08.

RESVD

Reserved: Set to zero

BCST

Broadcast Command Received: Set internally.

BUSY

Subsystem Busy: Set with a discrete pin or by writing to address 0 00 04.

SSFL

Subsystem Flag: Set with a discrete pin or by writing to address 0 00 02.

DBCA

Dynamic Bus Control Acceptance: Set with a discrete pin or by writing to address 0 00 01.

TF

Terminal Flag: Set with a discrete pin.

The status register is cleared and the external bits loaded on all commands except 'Transmit Status' and 'Transmit Last Command'. The external status bits (both discrete and programmable) must be valid 600 nS from the rising edge of NVCR for transmit commands and mode codes, and 250 nS from the rising edge of NDATA for the last data word in a receive message.

If discrete status inputs are not used they may be left open circuit.

STATUS RESPONSE TIME

The response time (all commands) measured from the mid bit zero crossing of the last bit of the last word to the mid bit zero crossing of the status word sync is nominally 11.0 µS.

This time period is used to monitor for more data words on the bus. If a valid sync field followed by four valid Manchester bi-phase bits are detected then this is considered to be another word on the bus.

The response time may be reduced to 6.0 µS (4.0 µS dead bus time) by setting the MCAIR input active high.

MESSAGE ILLEGALIZATION

Any command or mode command may be illegalised by setting the NME input active low. The remote terminal will respond with status with the Message Error bit set, provided the message was valid, and not use the information received. There will be no transfers to or from the memories.

One way to implement this function is to place a latching PROM to the T0-T10 data bus. The PROM would only have to decode 11 bits (5 bits subaddress, 5 bit word count and 1 bit T/R) and have a one bit output to place a high / low level on the NME input pin. The upper five bits (T11-T15) are just the Remote Terminal address for the unit which is constant so no decode of these bits is necessary. The latching signal for the PROM would be the NVCR line. The NME signal will remain latched and stable until the next rising edge of NVCR.

Reserved mode commands are automatically declared illegal by the device and need not be included in the PROM decode.

All other conditions which require the message error bit to be set are automatic.

DEVICE STATUS

The status of the device may be determined by reading from location 0 00 01. The subsystem programmable Remote Terminal status bits, Block Transfer Logic and Self Test status will be available on pins DATA 0-7.

| | |
|--------|----------------------------|
| DATA 0 | Dynamic Bus Control Accept |
| DATA 1 | Subsystem Flag |
| DATA 2 | Subsystem Busy |
| DATA 3 | Service Request |
| DATA 4 | BTL write enabled |
| DATA 5 | BTL read enabled |
| DATA 6 | Offline Self Test enabled |
| DATA 7 | Online Self Test enabled |

BIT REGISTER

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

DATA WRITTEN BY SUBSYSTEM

Writing data to 1 00 13 or 1 1F 13 (not McAir) will set the contents of the BIT register. The data may also be read from these locations. This register is not resettable.

The contents of the BIT register are transmitted onto the 1553 data bus following Status in response to the mode command "Transmit BIT word".

1760 CHECKSUM

The 1760 checksum logic is enabled by setting the input NENCHK active low.

For transmit messages the checksum word is generated and inserted in the last word position of the transmitted message.

For received messages the last data word receive (the checksum word) is validated. If this word meets the required criteria the output NVALCHK becomes valid on the falling edge of signal NCMDSTRB, and remains valid until the next NCMDSTRB of a receive message. This signal is only updated on valid receive commands as transmit commands do not require an incoming checksum validation.

In addition to the NVALCHK signal, an output STATUS is provided. This signal will toggle up and down for each data word received as it is calculating the checksum.

The open drain output (STATUS) signal may be hard wired to any of the discrete status inputs to set the required bit of the status response in the current message. In addition it may be hard wired to the input NILLCMD which will prevent the message being written to memory (e.g. if it is required to set the Service Request bit and not use the data for a failed checksum -hard wire STATUS to NSR and NILLCMD).

1760 HEADER WORD

In 1760 applications the first data word received is designated the header word. An output NHDR is provided to indicate the presence of this word on the highway T0-T15 for verification purposes. A failed header word may be treated in the same way as a failed checksum.

STORE RELEASED

The signal STREL is provided in 1760 applications to indicate to the subsystem that the store is no longer connected to the aircraft.

INITIALIZATION OF THE DEVICE

The device must be reset to a known state on power up. (If the LA input is high, the RT address will be latched). It will remain inactive until a valid command word is received. If the device is in the process of sequencing a command and a new command is received on the alternative bus, the sequence will be terminated and the device will sequence the new command.

The device will only consider a command word valid if the following conditions are met:-

- a) It contains the correct sync field.
- b) Correct Manchester bi-phase (16 bits plus parity).
- c) Correct parity (odd).
- d) Correct terminal address or broadcast address.
- e) Does not follow contiguously a valid word on the same bus.

The device will only consider a data word valid if the following conditions are met:-

- a) It contains the correct sync field.
- b) Correct Manchester bi-phase (16 bits plus parity).
- c) Correct parity (odd).
- d) Follows contiguously a valid word on the same bus.

Upon receipt of a valid command word the signal NVCR becomes active low for 500 nS. (The command word is available on T0-T15 during this period for message illegalization).

On all commands except 'Wrap Around Transmit' the 32 data word memory is cleared.

RT TO BC TRANSFER



If a valid command is received to transmit up to 32 data words the device will initially respond with Status.

The signal NCMDSTRB goes low indicating that a completely validated message has been received. The transmit Command word appears on T0-T15 at this time and is stored in the Command / Status memory causing NEMPTY to go high.

The end of the NCMDSTRB will initiate the DMA cycle to transfer the data words from the main RAM to the data buffer memory in a single burst at 1 μS per word. Data is transferred from the data buffer memory to the output buffer for transmission as required by the 1553 data bus.

The NCMDSTRB pulse is 8.5 μS long and during this time the bus arbitration logic is active. If the subsystem has already started an access to the main RAM before NCMDSTRB then it must complete before the end of NCMDSTRB. If the subsystem starts an access to the main RAM after the NCMDSTRB has begun the acknowledge (NACK) will not occur until after the DMA cycle has completed.

The Command word is used as the address pointer to the main RAM for reading data. This address is decremented by one to read the first data word for transmission, therefore the last data word transmitted is always read from the address location that has a word count field of zero.

| Error Conditions | Action taken by device |
|--------------------------------------|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| 3. Broadcast address. | No status response. Set message error. Set broadcast. Sequence terminated. |

BC TO RT TRANSFER



If a valid command is received to receive up to 32 data words and the second word is another command word then an RT to RT transfer has been set up (see RT to RT transfer).

All valid data words received are stored in the data buffer memory until message validation is complete after which the device will respond with Status. If the command was a broadcast the status transmission will be suppressed and the broadcast bit in the status register set.

Only after the message has been completely validated will the data be transferred to the main RAM in a single burst at 500 nS per word. This ensures that only complete validated messages are stored in the main RAM.

When a complete validated message is stored in the data buffer memory the signal NCMDSTRB goes low indicating that a completely validated message has been received. The received Command word appears on T0-T15 at this time and is stored in the Command / Status memory causing NEMPTY to go high.

The end of the NCMDSTRB will initiate the DMA cycle to transfer the data words from the data buffer memory to the main RAM. The NCMDSTRB pulse is 8.5 μS long and during this time the bus arbitration logic is active. If the subsystem has already started an access to the main RAM before NCMDSTRB then it must complete before the end of NCMDSTRB. If the subsystem starts an access to the main RAM after the NCMDSTRB has begun the acknowledge (NACK) will not occur until after the DMA cycle has completed.

The Command word is used as the address pointer to the main RAM for storing data. This address is decremented by one to store the first data word that was received, therefore the last data word received is always written to the address location that has a word count field of zero. The most significant bit of the address (bit 11) indicates that the Command received was a Broadcast and the data must be stored in the Broadcast area of RAM.

| Error Conditions | Action taken by device |
|-------------------------|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Invalid data word. | No status response. Set message error. Sequence terminated. |
| 3. Non contiguous data. | No status response. Set message error. Sequence terminated. |
| 4. Too few data words. | No status response. Set message error. Sequence terminated. |
| 5. Too many data words. | No status response. Set message error. Set broadcast. Sequence terminated. |

RT TO RT TRANSFER



To initiate an RT to RT transfer the Bus Controller will send a receive command to RTA followed contiguously by a transmit command to RTB.

RTB will respond with status and contiguous data (see RT to BC transfer).

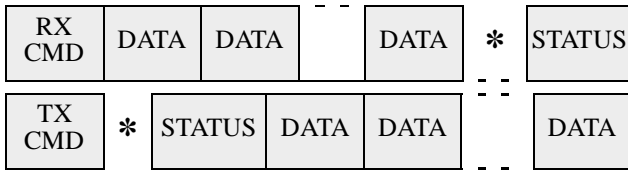
RTA (the receiving terminal) will receive the status and data transmitted by RTB and store the received data in the data buffer memory until the entire RT to RT transfer has been validated, after which it will respond with its own status provided it was not a broadcast command, in which case the status transmission will be suppressed and the broadcast bit set. It will then transfer the data to RAM (see BC to RT transfer).

Both the receiving and transmitting terminals will write their own commands to their Command / Status memories.

The error detection for the transmitting terminal will be the same as for RT to BC transfer. The error detection for the receiving terminal is as follows:-

| Error Conditions | Action taken by device |
|---|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Non contiguous command words. | No status response. Set message error. Sequence terminated. |
| 3. Transmit command followed by another word (excluding command word for RTA, in which case it will respond to the latest command). | No status response. Set message error. Sequence terminated. |
| 4. Transmitting terminal does not respond with status within 16 μS. | No status response. Set message error. Sequence terminated. |
| 5. Incorrect terminal transmitting. | No status response. Set message error. Sequence terminated. |
| 6. Non contiguous data following status from RTB. | No status response. Set message error. Sequence terminated. |
| 7. Invalid data transmitted from RTB. | No status response. Set message error. Sequence terminated. |
| 8. Too few or too many data words. | No status response. Set message error. Sequence terminated. |

WRAP AROUND



The wrap around capability is for test purposes only. It will test for transfers to and from the Bus Controller without any sub system intervention.

The wrap around sequence will commence on receipt of a valid receive command word containing the wrap around subaddress (1E) providing the WRAPEN input is set high. The data received is stored in the “transmit” area of the main RAM and the Command word is stored in the Command / Status memory as described in BC to RT transfer. The device will respond with status. The Bus Controller will then send a transmit command to subaddress 1E and the data contained in the “transmit” area of the main RAM will be transmitted following the status and the Command word which is stored in the Command / Status memory as described in RT to BC transfe

| Error Conditions | Action taken by device |
|---|---|
| RECEIVE | |
| 1. Invalid command. | No response. Command ignored. |
| 2. Invalid data word. | No status response. Set message error. Sequence terminated. |
| 3. Non contiguous data. | No status response. Set message error. Sequence terminated. |
| 4. Too few or too many data words. | No status response. Set message error. Sequence terminated |
| TRANSMIT | |
| 5. Invalid command. | No response. Command ignored. |
| 6. Command followed by another word. | No status response. Set message error. Sequence terminated |
| 7. Broadcast address. | No status response. Set message error. Set broadcast. Sequence terminated. |
| 8. Transmit word count not equal to receive word count. | No data transmission. Set message error. Sequence terminated. |

DYNAMIC BUS CONTROL (00)



The device will respond with status. If the terminal wishes to take over control of the bus, it must set the Dynamic Bus Control Acceptance bit of the status.

| Error Conditions | Action taken by device |
|---|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| 3. T/R bit of command set to zero. | No status response. Set message error. Sequence terminated |
| 4. Broadcast address. | No status response. Set message error. Set broadcast. Sequence terminated. |
| 5. T/R bit of command set to zero and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

SYNCHRONIZE WITHOUT DATA WORD (01)

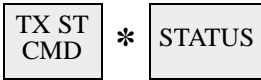


The device will respond with status. The NSYNC signal will go active low for 500 ns. Throughout this period the highway T0-T15 will be zero and remain at zero until the next command is received.

If the command was a broadcast the status transmission will be suppressed and the broadcast bit in the status register set.

| Error Conditions | Action taken by device |
|---|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| 3. T/R bit of command set to zero. | No status response. Set message error. Sequence terminated |
| 4. T/R bit of command set to zero and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

TRANSMIT STATUS (02)



The status register is not cleared or loaded before it is transmitted, i.e. it contains the resulting status from the previous command.

| Error Conditions | Action taken by device |
|---|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| 3. T/R bit of command set to zero. | No status response. Set message error. Sequence terminated. |
| 4. Broadcast address. | No status response. Set message error. Set broadcast. Sequence terminated. |
| 5. T/R bit of command set to zero and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

INITIATE SELF TEST (03)

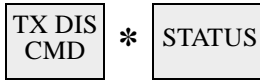


The device will respond with status. It is at the discretion of the subsystem whether or not to carry out a self test. A subsystem driven self test is contained within the unit.

If the command was a broadcast the status transmission will be suppressed and the broadcast bit in the status register set.

| Error Conditions | Action taken by device |
|---|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| 3. T/R bit of command set to zero. | No status response. Set message error. Sequence terminated. |
| 4. T/R bit of command set to zero and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

TRANSMITTER SHUTDOWN (04)



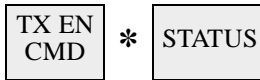
The device will respond with status and shutdown the transmitter on the alternate bus, thus inhibiting any further transmission on that bus.

Once a transmitter has been shutdown it can only be reactivated by the mode commands 'Override Transmitter Shutdown' or 'Reset Remote Terminal'.

If the command was a broadcast the status transmission will be suppressed and the broadcast bit in the status register set.

| Error Conditions | Action taken by device |
|---|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| 3. T/R bit of command set to zero. | No status response. Set message error. Sequence terminated. |
| 4. T/R bit of command set to zero and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

OVERRIDE TRANSMITTER SHUTDOWN (05)

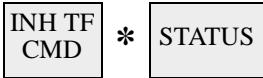


The device will respond with status and reactivate a shutdown transmitter on the alternate bus.

If the command was a broadcast the status transmission will be suppressed and the broadcast bit in the status register set.

| Error Conditions | Action taken by device |
|---|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| 3. T/R bit of command set to zero. | No status response. Set message error. Sequence terminated. |
| 4. T/R bit of command set to zero and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

INHIBIT TERMINAL FLAG (06)



The device will respond with status and then inhibit any further setting of the Terminal Flag bit of the status.

Once the Terminal Flag bit has been inhibited it can only be reactivated by the mode commands 'Override Inhibit Terminal Flag' or 'Reset Remote Terminal'.

If the command was a broadcast the status transmission will be suppressed and the broadcast bit in the status register set.

| Error Conditions | Action taken by device |
|---|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| 3. T/R bit of command set to zero. | No status response. Set message error. Sequence terminated |
| 4. T/R bit of command set to zero and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

OVERRIDE INHIBIT TERMINAL FLAG (07)

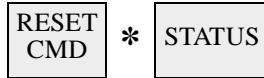


The device will respond with status and then reactivate the Terminal Flag bit of the status register.

If the command was a broadcast the status transmission will be suppressed and the broadcast bit in the status register set.

| Error Conditions | Action taken by device |
|---|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| 3. T/R bit of command set to zero. | No status response. Set message error. Sequence terminated |
| 4. T/R bit of command set to zero and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

RESET REMOTE TERMINAL (08)



The device will respond with status after which the bidirectional signal NRES to the subsystem will go active low for 500 ns.

Transmitter Shutdown mode commands and Inhibit Terminal Flag mode command will be reactivated.

The Command / Status memory will also be cleared.

If the command was a broadcast the status transmission will be suppressed and the broadcast bit in the status register set.

| Error Conditions | Action taken by device |
|---|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| 3. T/R bit of command set to zero. | No status response. Set message error. Sequence terminated |
| 4. T/R bit of command set to zero and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

RESERVED MODE CODES (09-0F)



The status is not cleared or loaded before it is transmitted with the message error bit set.

If the command was a broadcast the status transmission will be suppressed and the broadcast bit in the status register set.

| Error Conditions | Action taken by device |
|---|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| 3. T/R bit of command set to zero. | No status response. Set message error. Sequence terminated |
| 4. T/R bit of command set to zero and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

TRANSMIT VECTOR WORD (10)



On receipt of a valid Command to transmit the Vector Word the device will initially respond with Status. The Command word is written to the Command / Status memory at NVCR time causing the NEMPTY signal to go high.

After the Status response has been initiated the Vector Word will be read from RAM location 1 00 10 or 1 1F 10 depending on the Command subaddress and transferred to the Output Buffer ready for transmission onto the 1553 data bus following the Status.

The arbitration logic becomes active at NVCR time. If the subsystem has already started an access to the main RAM before NVCR then it must complete within 8 μS (3 μS if McAir response time is selected). If the subsystem starts an access to the main RAM after the NVCR has begun the acknowledge (NACK) will not occur until after the DMA cycle has completed which is approx 8 μS after NVCR (or 3 μS for McAir).

| Error Conditions | Action taken by device |
|---|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| 3. T/R bit of command set to zero. | No status response. Set message error. Sequence terminated. |
| 4. Broadcast address. | No status response. Set message error. Set broadcast. Sequence terminated. |
| 5. T/R bit of command set to zero and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

SYNCHRONIZE WITH DATA WORD (11)



The Synchronize data word received is stored in the data buffer memory until message validation is complete after which the device will respond with Status. If the command was a broadcast the status transmission will be suppressed and the broadcast bit in the status register set. The Command word is written to the Command / Status memory at NVCR time causing the NEMPTY signal to go high.

After the Status response has been initiated the Synchronize Word will be written to RAM location 1 00 11 or 1 1F 11 depending on the Command subaddress during which time the NSYNC signal will go active low for 500 nS. T0-T15 will be set to the data word received throughout the NSYNC pulse.

The arbitration logic becomes active at NVCR time. If the subsystem has already started an access to the main RAM before NVCR then it must complete within 28 μS (23 μS if McAir response time is selected). If the subsystem starts an access to the main RAM after the NVCR has begun the acknowledge (NACK) will not occur until after the DMA cycle has completed which is approx 28 μS after NVCR (or 23 μS for McAir).

| Error Conditions | Action taken by device |
|--|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command not followed contiguously by data word | No status response. Set message error. Sequence terminated. |
| 3. Command followed by too many words. | No status response. Set message error. Sequence terminated. |
| 4. T/R bit of command set to one. | No status response. Set message error. Sequence terminated. |
| 5. T/R bit of command set to one and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

TRANSMIT LAST COMMAND (12)



The status response contains the resulting status from the previous command.

The data word transmitted following the status word contains the previous valid command (provided it was not Transmit Last Command).

| Error Conditions | Action taken by device |
|---|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| 3. T/R bit of command set to zero. | No status response. Set message error. Sequence terminated. |
| 4. Broadcast address. | No status response. Set message error. Set broadcast. Sequence terminated. |
| 5. T/R bit of command set to zero and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

TRANSMIT BIT WORD (13)



On receipt of a valid Command to transmit the BIT Word the device will initially respond with Status.

After the Status response has been initiated the Bit Word will be read from the BIT register and transferred to the Output Buffer ready for transmission onto the 1553 data bus following the Status.

The contents of the BIT register are set by the subsystem writing data to address 1 00 13 or 1 1F 13.

The bus arbitration logic is not required to become active for this mode command.

| Error Conditions | Action taken by device |
|---|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| 3. T/R bit of command set to zero. | No status response. Set message error. Sequence terminated. |
| 4. Broadcast address. | No status response. Set message error. Set broadcast. Sequence terminated. |
| 5. T/R bit of command set to zero and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

SELECTED TRANSMITTER SHUTDOWN (14)



This mode command is not normally used in dual redundant systems.

The device will respond with status and shut down the transmitter on the bus designated by the two least significant bits of the data word.

The bus addresses of the device are channel 0 - 00, channel 1 - 01. If the command is received on the same bus as the designated shut down bus then the device will respond with status and no shut down will occur.

Once a transmitter has been shut down it can only be reactivated by an 'Override Shutdown Command' or 'Reset Remote Terminal'.

If the command was a broadcast the status transmission will be suppressed and the broadcast bit in the status register set.

| Error Conditions | Action taken by device |
|--|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command not followed contiguously by data word | No status response. Set message error. Sequence terminated. |
| 3. Command followed by too many words. | No status response. Set message error. Sequence terminated. |
| 4. T/R bit of command set to one. | No status response. Set message error. Sequence terminated. |
| 5. T/R bit of command set to one and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

OVERRIDE SEL TRANSMITTER SHUTDOWN (15)



This mode command is not normally used in dual redundant systems.

The device will respond with status and reactivate a shutdown transmitter on the bus designated by the two least significant bits of the data word.

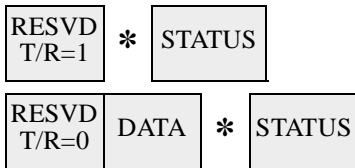
The bus addresses of the device are channel 0 - 00 channel

1 - 01. If the command is received on the same bus as the designated override shutdown bus then the device will respond with status and no reactivation will occur.

If the command was a broadcast the status transmission will be suppressed and the broadcast bit in the status register set.

| Error Conditions | Action taken by device |
|--|---|
| 1. Invalid command. | No response. Command ignored. |
| 2. Command not followed contiguously by data word | No status response. Set message error. Sequence terminated. |
| 3. Command followed by too many words. | No status response. Set message error. Sequence terminated. |
| 4. T/R bit of command set to one. | No status response. Set message error. Sequence terminated. |
| 5. T/R bit of command set to one and broadcast address | No status response. Set message error. Set broadcast. Sequence terminated. |

RESERVED MODE CODES (16-1F)



The status is not cleared or loaded before it is transmitted with the message error bit set.

If the command was a broadcast the status transmission will be suppressed and the broadcast bit in the status register set.

| Error Conditions | Action taken by device |
|--|---|
| T/R = 1 | |
| 1. Invalid command. | No response. Command ignored. |
| 2. Command followed by another word. | No status response. Set message error. Sequence terminated. |
| T/R = 0 | |
| 3. Invalid command. | No response. Command ignored. |
| 4. Command not followed contiguously by data word. | No status response. Set message error. Sequence terminated. |
| 5. Command followed by too many data words. | No status response. Set message error. Sequence terminated. |

BUS CONTROLLER OPERATION

Writing to address 1 00 01 will set the device up as a Bus Controller.

TRANSMIT COMMAND

The command word to be transmitted on the bus should be written to address 0 00 00. The device performs the following functions:-

- a) Transmits Command word.
- b) Load command word into address pointer.

Upon receipt of a fully validated message the device performs the following functions:-

- c) Write the Remote Terminals Status response word into the Command / Status memory. If the Busy bit is set the sequence is terminated.
- d) Switch the RAM to 1553 mode.
- e) Write data words to RAM and decrement address until zero.
- f) Switch RAM back to processor access.

RECEIVE COMMAND

Prior to issuing the Command word the appropriate RAM locations should be updated to contain the data for transmission. The Command word to be transmitted is then written to address 0 00 00. The device performs the following functions:

- a) Transmits Command word.
- b) Load command word into address pointer.
- c) Switch the RAM to 1553 mode.
- d) Transfer data words from main RAM to data buffer memory, transmit data and decrement address until zero.
- e) Switch RAM back to processor access.
- f) Writes the Remote Terminals Status response word into the Command / Status memory.

RT TO RT TRANSFER

- a) The first command (the receive command) to be transmitted on the Data Bus is written to address 0 00 01.
- b) The command word is transmitted.
- c) The second command (the transmit command) is written to address 0 00 00.
- d) This command is transmitted.
- e) The two Status response words are written into the Command / Status memory.

MODE CODES WITHOUT DATA

- a) The command word to be transmitted on the data bus should be written to address 0 00 00.
- b) The command word is transmitted.
- c) The Status response word is written to the Command / Status memory.

MODE CODES WITH DATA (TRANSMIT)

These mode commands are:-

| | |
|-----------------------|--------------------|
| Transmit Vector Word | 1 00 10 or 1 1F 10 |
| Transmit Last Command | 1 00 12 or 1 1F 12 |
| Transmit BIT Word | 1 00 13 or 1 1F 13 |

The command word to be transmitted on the bus should be written to address 0 00 00. The device performs the following functions:-

- a) Transmits command word.
- b) Load command word into address pointer.

Upon receipt of a fully validated message the device performs the following functions:-

- c) Write the Status response word into the Command / Status memory.
- d) Switch the RAM to 1553 mode.
- e) Write the data word to RAM.
- f) Switch RAM back to processor access.

MODE CODES WITH DATA (RECEIVE)

These mode commands are:-

| | |
|---|--------------------|
| Synchronize with data word | 0 00 11 or 0 1F 11 |
| Selected Transmitter Shutdown Bus 0 | 0 00 14 or 0 1F 14 |
| Selected Transmitter Shutdown Bus 1 | 0 00 14 or 0 1F 14 |
| Override Sel Transmitter Shutdown Bus 0 | 0 00 15 or 0 1F 15 |
| Override Sel Transmitter Shutdown Bus 1 | 0 00 15 or 0 1F 15 |

Prior to issuing the mode code the relevant RAM location should be updated with the data word to be transmitted.

The command word to be transmitted on the Data Bus should be written to address 0 00 00. The device performs the following functions:-

- a) Transmits command word.
- b) Load command word into address pointer.
- c) Switch the RAM to 1553 mode.
- d) Transmits the data word from the RAM location specified above.
- e) Switch RAM back to processor access.
- f) Write the Remote Terminals status word into the Command / Status memory.

8 BIT INTERFACE

With input NBIT16 high, an 8 bit processor interface has been selected. In this mode, signals DATA8 to DATA15 are unused.

The upper byte is read/written via signals DATA0 to DATA7.

Input "UB" controls the access to the upper and lower bytes and must be asserted along with the address highway.

UB = 1 select upper byte

UB = 0 select lower byte

Input UB may form part of the address highway and is inverted in Multibus mode. The upper byte of a word must always be accessed before the lower byte. All timing information is the same for a 16 bit interface.

BUS CONTROLLER DETAIL

BUS SELECT

The bus that messages are transmitted on is selected by writing to address 0 00 10 for bus 0, and 0 00 11 for bus 1. Once selected, messages will be transmitted on the chosen bus until the alternate bus is selected.

ERROR HANDLING

There are two separate groups of error detected.

- a) Errors between the host and the device.
- b) Errors on the Data Bus.

If an error is detected the ERROR signal goes active high terminating the current Bus Control sequence and the error register will indicate the nature of the error. The Error contents are accessed by reading from RAM location 0 00 12.

ERROR REGISTER

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

DATA WRITTEN BY BUS CONTROL PROTOCOL

- 0 Error in command transferred to the device - command will not be transmitted.
- 1 Error in RT to RT commands transferred to the device - first command may not be transmitted, second command will not be transmitted.
- 2 Illegal command transferred to device - command will not be transmitted.
- 3 Illogical command transferred to device - command will not be transmitted.

- 4 Illegal broadcast command transferred to device - command will not be transmitted.
- 5 Error in word count fields of RT to RT commands transferred to device.
- 6 Set to zero.
- 7 Error in message transfer on the data bus.
- 8 Too few valid data words transferred on the data bus or non contiguous data.
- 9 Too many words transferred on the data bus.
- 10 No valid status response on the data bus.
- 11 Incorrect RT responding to command or first command in RT to RT transfer.
- 12 Incorrect RT responding to second command in RT to RT transfer.
- 13-15 Set to zero.

On receipt of the ERROR signal the devices takes the following action:-

- a) Switch the RAM to 1553 mode.
- b) Enable the Error register.
- c) Transfer the contents of the Error register to RAM location 0 00 12.
- d) Disable the Error register.
- e) Switch RAM back to processor access.

The contents of the RAM location 0 00 12 are only updated upon receipt of an error.

END OF TRANSFER

The background processor should use the signal EOT from the device to determine when the current data bus transaction has successfully completed. The processor should read the Status word / words from the Command / Status memory in addition to the Error word from RAM.

1760 CHECKSUM

The 1760 checksum logic is enabled by setting the input NENCHK active low.

For BC to RT messages the checksum word is generated and inserted in the last word position of the transmitted message.

For RT to BC messages the last data word received (the checksum word) is validated. If this word meets the required criteria the output NVALCHK becomes valid on the falling edge of signal NSTSTRB, and remains valid until the next NSTSTRB of a transmit message. This signal is only updated on valid transmit commands as receive commands do not require an incoming checksum validation.

In addition to the NVALCHK signal, an output STATUS is provided. This signal will toggle up and down for each data word received as it is calculating the checksum.

The open drain output (STATUS) signal may be hard wired to the input NINHST which will illegalise a message just received and prevent any data received being transferred to the main RAM, the Status word will not be stored in the Command / Status memory.

MCAIR

If the McAir function is selected, a subaddress field of 1F will be treated as a non mode command.

RT TO BC TRANSFER



The Transmit Command word is written to address 0 00 00 after which it is transmitted onto the 1553 data bus.

All valid data words received are stored in the data buffer memory until message validation is complete. Only after the message has been completely validated will the data be transferred to the main RAM in a single burst at 1 μ S per word. This ensures that only complete validated messages are stored in the main RAM.

When a complete validated message is stored in the data buffer memory the signal NSTSTRB goes low indicating that a completely validated message has been received. The Status Response word appears on T0-T15 at this time and is stored in the Command / Status memory causing NEMPTY to go high.

If the Busy bit in the Status response is set their will be no associated data therefore no DMA transfer will take place.

The end of the NSTSTRB will initiate the DMA cycle to transfer the data words from the data buffer memory to the main RAM. The NSTSTRB pulse is 8.5 μ S long and during this time the bus arbitration logic is active. If the subsystem has already started an access to the main RAM before NSTSTRB then it must complete before the end of NSTSTRB. If the subsystem starts an access to the main RAM after the NSTSTRB has begun the acknowledge (NACK) will not occur until after the DMA cycle has completed.

The Command word is used as the address pointer to the main RAM for storing data. This address is decremented by one to store the first data word that was received, therefor the last data word received is always written to the address location that has a word count field of zero.

| Error Conditions | Action taken by device |
|---|--|
| 1. Broadcast command. | Set error bits 0, 4. Set Error. Set end of transfer. Sequence terminated. Command not transmitted. |
| 2. RT response time greater than 16 μ S. | Set error bit 10. Set Error. Set end of transfer. Sequence terminated. |
| 3. Incorrect RT responding. | Set error bit 11. Set Error. Sequence terminated |
| 4. Sync, biphase or parity error in data, or too few data words received, or non contiguous data. | Set error bits 7, 8. Set Error. Set end of transfer. Sequence terminated. |
| 5. Too many data words received. | Set error bits 7, 9. Set Error. Sequence terminated |

BC TO RT TRANSFER



Data for transmission must be available in the main RAM prior to initiating a BC to RT transfer.

The Receive Command word is written to address 0 00 00 after which it is transmitted onto the 1553 data bus.

The end of write to 0 00 00 will initiate the DMA cycle to transfer the data words from the main RAM to the data buffer memory in a single burst at 1 μ S per word. Data is transferred from the data buffer memory to the output buffer for transmission as required by the 1553 data bus.

If the subsystem starts an access to the main RAM during this DMA transfer the acknowledge (NACK) will not occur until after the DMA cycle has completed.

The Command word is used as the address pointer to the main RAM for reading data. This address is decremented by one to read the first data word for transmission, therefor the last data word transmitted is always read from the address location that has a word count field of zero. If the Remote Terminals address field of the Command word was set to 1F (Broadcast) then the data will be read from the Broadcast area of RAM.

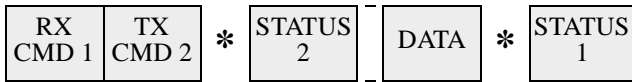
When a complete validated message has been received by the Remote Terminal it will respond with its Status. When the Bus Controller receives a valid Status Response the signal NSTSTRB goes low for 8.5 μ S. The Status Response word appears on T0-T15 at this time and is stored in the Command / Status memory causing NEMPTY to go high.

If the Command was a Broadcast there will be no Status response therefore signal NSTSTRB will not become active.

There is no bus arbitration requirement when writing the Status word to the Command / Status memory.

| Error Conditions | Action taken by device |
|---|---|
| 1. RT response time greater than 16 μ S (not broadcast) | Set error bit 10. Set Error. Set end of transfer. Sequence terminated. |
| 2. Incorrect RT responding. | Set error bit 11. Set Error. Sequence terminated. |
| 3. Status word followed by another word. | Set error bits 7, 9. Set Error. Sequence terminated |

RT TO RT TRANSFER



The first word to be transmitted (the receive command) is written to address 0 00 01. The second word (the transmit command) is then written to address 0 00 00.

On completion of a valid transfer from the transmitting terminal the signal NSTSTRB goes low for 8.5 μ S during which time the Status of the transmitting terminal is available on T0-T15. This Status word is written to the Command / Status memory. The transmitted data is not stored in the Bus Controllers RAM.

For non broadcast transfers the receiving terminal will respond with its Status and the signal NSTSTRB will once again go low for 8.5 μ S during which time the Status of the receiving terminal is available on T0-T15. This Status word is written to the Command / Status memory.

| Error Conditions | Action taken by device |
|--|--|
| 1. Command 1 - transmit or mode command. Command 2 - receive or mode command. | Set error bits 1, 3. Set Error. Sequence terminated. |
| 2. RT address command 1 same as RT address command 2. | Set error bits 1, 2. Set Error. Sequence terminated. |
| 3. Word count command 1 different from word count command 2. | Set error bits 1, 5. Set Error. Sequence terminated |
| 4. Command 2 broadcast. | Set error bits 1, 4. Set Error. Sequence terminated. |
| 5. RT 2 does not respond with status within 16 μ S. | Set error bit 10. Set Error. Set end of transfer. |
| 6. Incorrect RT responding to command 2. | Set error bits 12. Set Error. Sequence terminated. |
| 7. Sync, biphasic or parity error in data, or too few data words received, or non contiguous data. | Set error bits 7, 8. Set Error. Set end of transfer. Sequence terminated. |
| 8. Too many data words transferred. | Set error bits 7, 9. Set Error. Sequence terminated |
| 9. RT 1 does not respond with status within 16 μ S (non broadcast). | Set error bit 10. Set Error. Set end of transfer. Sequence terminated |
| 10. Incorrect RT responding to command 1. | Set error bits 11. Set Error. Sequence terminated. |
| 11. Status 1 followed by another word. | Set error bits 7, 9. Set Error. Sequence terminated. |

DYNAMIC BUS CONTROL (00)



The mode command word is written to address 0 00 00 after which it is transmitted onto the 1553 data bus.

When the Bus Controller receives a valid Status Response the signal NSTSTRB goes low for 8.5 μ S. The Status Response word appears on T0-T15 at this time and is stored in the Command / Status memory causing NEMPTY to go high.

If bit 1 of the status response (Dynamic Control Acceptance) is set, the device must relinquish control of the data bus. No more commands must be written to the device.

| Error Conditions | Action taken by device |
|--|--|
| 1. Broadcast command. | Set error bits 0, 4. Set Error. Set end of transfer. Sequence terminated. Command not transmitted. |
| 2. T/R bit of command set to zero. | Set error bits 0, 3. Set Error. Set end of transfer. Sequence terminated. Command not transmitted. |
| 3. RT response time greater than 16 μ S. | Set error bit 10. Set Error. Set end of transfer. Sequence terminated. |
| 4. Incorrect RT responding. | Set error bit 11. Set Error. Sequence terminated. |
| 5. Status word followed by another word. | Set error bits 7, 9. Set Error. Sequence terminated |

TRANSMIT STATUS (02)



The mode command word is written to address 0 00 00 after which it is transmitted onto the 1553 data bus.

When the Bus Controller receives a valid Status Response the signal NSTSTRB goes low for 8.5 μ S. The Status Response word appears on T0-T15 at this time and is stored in the Command / Status memory causing NEMPTY to go high.

This sequence applies to the following mode commands without an associated data word.

| Error Conditions | Action taken by device |
|--|--|
| 1. Broadcast command. | Set error bits 0, 4. Set Error. Set end of transfer. Sequence terminated. Command not transmitted. |
| 2. T/R bit of command set to zero. | Set error bits 0, 3. Set Error. Set end of transfer. Sequence terminated. Command not transmitted. |
| 3. RT response time greater than 16 μ S. | Set error bit 10. Set Error. Set end of transfer. Sequence terminated. |
| 4. Incorrect RT responding. | Set error bit 11. Set Error. Sequence terminated. |
| 5. Status word followed by another word. | Set error bits 7, 9. Set Error. Sequence terminated |

MODE COMMANDS 01 AND 03 TO 08

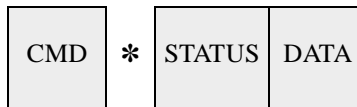
- 01 Synchronize
- 03 Initiate Self Test
- 04 Transmitter Shutdown
- 05 Override Transmitter Shutdown
- 06 Inhibit Terminal Flag Bit
- 07 Override Inhibit Terminal Flag Bit
- 08 Reset Remote Terminal



| Error Conditions | Action taken by device |
|---|--|
| 1. T/R bit of command set to zero. | Set error bits 0, 3. Set Error. Set end of transfer. Sequence terminated. Command not transmitted. |
| 2. RT response time greater than 16 μ S (not broadcast) | Set error bit 10. Set Error. Set end of transfer. Sequence terminated. |
| 3. Incorrect RT responding. | Set error bit 11. Set Error. Sequence terminated. |
| 4. Status word followed by another word. | Set error bits 7, 9. Set Error. Sequence terminated |

MODE COMMANDS 10,12,13

- 10 Transmit Vector Word
- 12 Transmit Last Command
- 13 Transmit Bit Word



The transmit mode command word is written to address 0 00

The valid data word received is stored in the data buffer memory until message validation is complete. Only after the message has been completely validated will the data be transferred to the main RAM. This ensures that only complete validated messages are stored in the main RAM.

When the message has been validated the signal NSTSTRB goes low. The Status Response word appears on T0-T15 at this time and is stored in the Command / Status memory causing NEMPTY to go high.

The end of the NSTSTRB will initiate the DMA cycle to transfer the data word from the data buffer memory to the main RAM. The NSTSTRB pulse is 8.5 μ S long and during this time the bus arbitration logic is active. If the subsystem has already started an access to the main RAM before NSTSTRB then it must complete before the end of NSTSTRB. If the subsystem starts an access to the main RAM after the NSTSTRB has begun the acknowledge (NACK) will not occur until after the DMA cycle has completed.

| Error Conditions | Action taken by device |
|---|--|
| 1. Broadcast command. | Set error bits 0, 4. Set Error. Set end of transfer. Sequence terminated. Command not transmitted. |
| 2. T/R bit of command set to zero. | Set error bits 0, 3. Set Error. Set end of transfer. Sequence terminated. Command not transmitted. |
| 3. RT response time greater than 16 μ S. | Set error bit 10. Set Error. Set end of transfer. Sequence terminated. |
| 4. Incorrect RT responding. | Set error bit 11. Set Error. Sequence terminated. |
| 5. Valid data word not received or non contiguous data. | Set error bits 7, 9. Set Error. Set end of transfer. Sequence terminated. |
| 6. Too many data words received. | Set error bits 7, 9. Set Error. Sequence terminated. |

MODE COMMANDS 11, 14, 15

- 11 Synchronize with Data Word
- 14 Selected Transmitter Shutdown
- 15 Override Selected Transmitter Shutdown



Data for transmission must be available in the main RAM prior to initiating a BC to RT transfer.

The receive mode command word is written to address 0 00 00 after which it is transmitted onto the 1553 data bus.

The end of write to 0 00 00 will initiate the DMA cycle to transfer the data word from the main RAM to the output buffer in 1 μS for transmission as required by the 1553 data bus.

If the Remote Terminals address field of the Command word was set to 1F (Broadcast) then the data will be read from the Broadcast area of RAM.

When a complete validated message has been received by the Remote Terminal it will respond with its Status. When the Bus Controller receives a valid Status response the signal NSTSTRB goes low for 8.5 μS. The Status response word appears on T0-T15 at this time and is stored in the Command / Status memory causing NEMPTY to go high.

If the Command was a Broadcast there will be no Status response therefore signal NSTSTRB will not become active.

| Error Conditions | Action taken by device |
|--|--|
| 1. T/R bit of command set to one. | Set error bits 0, 3. Set Error. Set end of transfer. Sequence terminated. Command not transmitted. |
| 2. RT response time greater than 16 μS (not broadcast) | Set error bit 10. Set Error. Set end of transfer. Sequence terminated. |
| 3. Incorrect RT responding. | Set error bit 11. Set Error. Sequence terminated. |
| 4. Status word followed by another word. | Set error bits 7, 9. Set Error. Sequence terminated |

RESERVED MODE COMMANDS 09 to 0F and 16 to 1F

If a reserved mode command is transferred to the device then the following action will be taken:-

1. Set error bits 0,2.
2. Set Error.
3. Set end of transfer.
4. Sequence terminated.
5. Command not transmitted.

BLOCK TRANSFER LOGIC

The Block Transfer Logic (BTL) may be enabled for both Remote Terminal and Bus Controller.

The BTL consists of a 32 word memory buffering the subsystem to the main RAM thus guaranteeing data consistency for both transmit and receive transfers.

All reads and writes to the BTL are identical to read / write to the main RAM. The address locations are the same. The only difference is that the BTL circuitry will intercept those read / writes and store them in the buffer instead. The user accesses the same locations as if they would if they were directly accessing the main RAM.

The block transfer logic is enabled with signal NENBTL(pin A7) being active low and is not applicable to subaddress 00 and 1F (unless McAir is selected) areas of ram. The block transfer logic may also be configured by writing to certain address locations providing NENBTL is selected, ie.

| | | |
|---------|---------------|--------------|
| 1 00 02 | Disable Write | Disable Read |
| 1 00 03 | Enable Write | Disable Read |
| 1 00 04 | Disable Write | Enable Read |
| 1 00 05 | Enable Write | Enable Read |

Reset will enable both Write and Read.

WRITE

The Write BTL Logic basically stores all writes to a particular subaddress in the buffer until the subsystem has completed the entire subaddress update. When the subsystem has finished, the BTL will generate a burst DMA from the BTL to main RAM in one contiguous transfer. This guarantees that the entire subaddress is updated. Until the DMA transfer the BTL buffer allows the main RAM to be free for updates from the 1553 data bus.

The user must write data to the device in a specific sequence starting with the first word for transmission in the n-1 location and ending with the last word for transmission in location 00 of the subaddress. The BTL will sense the write to location 00 and initiate the DMA sequence.

1. Data for one message is written to the 32 word buffer memory at any speed by the subsystem. The first word for transmission is written first to the n-1 location and the last word for transmission is written last to the 00 location of the subaddress.
2. The address of the first word is stored in a register / counter within the "block transfer logic".
3. The last word for transmission is always written to location zero, this will trigger the transfer of data from the 32 word buffer memory to the main memory. Data is transferred at the rate of 250 nS per word. A full 32 word transfer will take approx 8 μS.
4. If the 1553 is quiet the entire message will immediately be transferred in a single burst to the main memory, the address being generated by the counter within the block transfer logic. During this transfer the subsystem will be locked out via NACK from any new updates.

5. If the 1553 DMA transfer to the main RAM becomes active during the burst transfer, the transfer will complete and then be locked out of any new updates until the 1553 is complete. However the BTL buffer memory will be accessible to the subsystem at this time.
6. If the 1553 DMA transfer to the main RAM becomes active before the start of the burst transfer, the transfer will be locked out (after location zero is written to) until the 1553 is complete. The sub system will be locked out during this time (main ram being accessed by the 1553 and the BTL buffer memory is full). If the BTL memory is not fully loaded, the subsystem can continue to load the BTL memory until full (write to 00 indicates a full condition). When the 1553 is complete the burst transfer will take place and then unlock the subsystem.
7. Once the burst transfer has commenced it will complete, thus ensuring data consistency.

READ

The Read BTL functions similarly to the Write BTL in that the BTL buffers the read activity. A subsystem read will initially generate a DMA of that entire portion of the subaddress to be stored in the BTL buffer. The subsystem can then read out the data at its leisure while the main RAM is free for future updates. Since the entire portion of the subaddress data was DMA from the RAM, the data read from the BTL buffer is guaranteed contiguous.

The user must read data from the device in a specific sequence starting with the first word received in the n-1 location and ending with the last word received in location 00 of the subaddress. The BTL will sense the read from location 00 and reset the sequence ready for a new access.

1. The first word of a received message will be read first, this will initiate a burst DMA transfer of a complete message from main memory to the 32 word BTL buffer memory, during which time the subsystem will be locked out. Data is transferred at the rate of 250 ns per word.
2. The sub system can then read data from the ram at its leisure. The last word to be read will be the last word received in the message and read from location zero. This will reset the block transfer logic.
3. If the 1553 DMA transfer to the main RAM becomes active during the burst transfer, the transfer will complete and then be locked out until the 1553 is complete. However the 32 word BTL buffer memory will be accessible to the subsystem at this time to read out the data.
4. If the 1553 DMA transfer to the main RAM becomes active before the start of the burst transfer, the transfer will be locked out until the 1553 is complete. The sub system will be locked out during this time (main ram being accessed by the 1553 and the 32 word buffer memory is waiting for the receive message). When the 1553 is complete the burst transfer will take place and then unlock the subsystem.
5. Once the burst transfer has commenced it will complete, thus ensuring data consistency.

SELF TEST

The self test feature is an internal and external loop back test for additional verification of functionality. This is in addition to the Remote Terminal Wraparound circuitry. The difference is that this test is manual and under subsystem control. The subsystem microprocessor initiates the self test and the subsequent data word pattern. The subsystem then reads back the wrapped data word and determines if it is correct. The online self test must be done with the 1553 data bus quiet.

The self test function is enabled or disabled by writing to certain address locations. Reset will disable self test.

| | |
|---------|--|
| 1 00 06 | Enable offline self test and set device status bit 6 |
| 1 00 07 | Enable online self test and set device status bit 7 |
| 1 00 08 | Disable self test |

When self test is enabled the device is set up as both BC and RT. When self test is disabled the device will revert back to its previous state.

BASIC OPERATION

The basic operation is for the BC to transmit the message "receive one data word" and for the RT to receive this message.

If the online self test is selected the message will be transmitted onto the 1553 bus via the transceivers and be received by the RT via transceivers. The RT will not respond with Status.

If the offline self test is selected the transceivers will be inhibited and the Manchester encoder output is routed to the Manchester decoder input.

The status of the device may be obtained by reading from 0 00 01. Bit 6 is offline self test enabled. Bit 7 is online self test enabled.

DETAILED OPERATION

1. Enable self test by writing to either 1 00 06 (offline) or 1 00 07 (online).
2. Select required 1553 data bus to be tested by writing to 0 00 10 or 0 00 18.
3. Write the data word contents required for the self test to the appropriate RAM location ie. For broadcast message: 2(bcast) 01-1E(subaddress) 00(1 word) or normal receive message: 0(rec) 01-1E(subaddress) 00(1 word).
4. Initiate BC to RT transfer of one data word by writing to address 0 00 00 with a data word content of 1F or RTaddr 0(rec) 01-1E(subaddress) 01(1 data word). The following automatic sequence is now initiated:-
 - a) The Command word (data word written to location 0 00 00) is processed by the BC protocol, transferred to the Manchester encoder and transmitted onto the bus (online self test) or to the Manchester decoder (offline self test).
 - b) The self test data word is read from the appropriate RAM location, transferred to the encoder and transmitted contiguously following the command word.
 - c) The Command word is received by the Manchester decoder, if valid and with correct RT address or broadcast is stored in the RT protocol.

- d) The data word is received by the decoder and if valid is stored in the 32 word data memory.
 - e) The RT protocol will validate the message and if successful will write the Command word to the 32 word Command / Status memory and transfer the data word to the appropriate RAM location.
5. As the data word received is written to the same RAM location that it was originally accessed from, the contents should be altered while the self test is in progress (eg. write 0000). This can be done immediately after the BC to RT transfer was initiated. There is approx 45 µS for the self test to complete.
 6. To ensure that the RAM contents have been altered it is advisable to read the data back from the RAM.
 7. On completion of a successful self test the signal NCMDSTRB will go active low, after which the data can be read from the RAM and compared with the data used in the self test.
 8. In addition the Command word used in the self test may be read from 0 00 00.
 9. Disable self test by writing to 1 00 08. The device will revert back to its original state (BC or RT).

3. ADDR = 2 01-1E 00 (Write) Write self test data to location.
DATA = n
- or ADDR = 0 01-1E 00 (Write) Write self test data to REC location.
DATA = n
4. ADDR = 0 00 00 (Write) Transmit message (Bcast rec 1 word).
DATA = 1F 0 01-1E 01
- or ADDR = 0 00 00 (Write) Transmit message (Rec 1 word).
DATA = RTAD 0 01-1E 01
5. ADDR = 2 01-1E 00 (Write) Write 0 to self test location.
DATA = 0
- or ADDR = 0 01-1E 00 (Write) Write 0 to self test location.
DATA = 0
6. ADDR = 2 01-1E 00 (Read) Read 0 from self test location.
DATA = 0
- or ADDR = 0 01-1E 00 (Read) Read 0 from self test location.
DATA = 0
7. ADDR = 2 01-1E 00 (Read) Read self test data after NCMDSTRB.
DATA = n
- or ADDR = 0 01-1E 00 (Read) Read self test data after NCMDSTRB.
DATA = n
8. ADDR = 0 00 00 (Read) Read command from command memory.
DATA = 1F 0 01-1E 01
- or ADDR = 0 00 00 (Read) Read command from command memory.
DATA = RTAD 0 01-1E 01
9. ADDR = 1 00 08 (Write) Disable self test.
- ADDR = 0 00 01 (Read) Read device status:
Bit 6 = Offline self test.
Bit 7 = Online self test.

SUMMARY OF OPERATION

Device can be either RT or BC.

1. ADDR = 1 00 06 (Write) Select offline self test.
or ADDR = 1 00 07 (Write) Select online self test.
2. ADDR = 1 00 10 (Write) Select bus 0.
or ADDR = 1 00 18 (Write) Select bus 1.

DEVICE MEMORY MAP

Subaddress 00 and 1F of the memory block areas are designated as mode code operations by the MIL-STD-1553 bus. Therefore, these locations can be used for control registers. Any area outside the control registers in these subaddresses are just general unused memory locations. Address locations are listed in hex and in five bit address fields for simplicity in correlating to MIL-STD-1553 commands.

REMOTE TERMINAL

| Address | Data | Function / Comments | Reset |
|--|---|---|--------------|
| 0 00 00 * Read | Command received by RT | Read Command Memory | |
| 0 00 00 * Write 0 00 01 * Write 0 00 02 * Write 0 00 03 * Write 0 00 04 * Write 0 00 05 * Write 0 00 06 * Write 0 00 07 * Write 0 00 08 * Write 0 00 09 * Write 0 00 0A * Write 0 00 0B * Write 0 00 0C * Write 0 00 0D * Write 0 00 0E * Write 0 00 0F * Write | X X X X X X X X X X X X X X X X X | Clear status Status = DBCA Status = SSFLAG Status = SSFLAG+DBCA Status = BUSY Status = BUSY+DBCA Status = BUSY+SSFLAG Status = BUSY+SSFLAG+DBCA Status = SR Status = SR+ DBCA Status = SR+ SSFLAG Status = SR+ SSFLAG+DBCA Status = SR+ BUSY Status = SR+ BUSY+DBCA Status = SR+ BUSY+SSFLAG Status = SR+ BUSY+SSFLAG+DBCA | Clear Status |
| 0 00 01 * Read | Status (bits 0-7) | Read status | |

REMOTE TERMINAL con't

| Address | Data | Function / Comments | Reset |
|--|-------------------------------|--|---------|
| 0 00 11 Read | Synchronize word | Synchronize with data mode code | |
| 0 01 n to Read 0 1E n | Data received by RT | First data word Address = n-1 Last data word Address = 0 | |
| 0 1F 11 Read | Synchronize word | Synchronize with data mode code | |
| 1 00 00 Write 1 00 01 Write | X X | Select RT Select BC | RT |
| 1 00 02 * Write 1 00 03 * Write 1 00 04 * Write 1 00 05 * Write | X X X X | Disable BTL write Disable BTL read Enable BTL write Disable BTL read Disable BTL write Enable BTL read Enable BTL write Enable BTL read | Enable |
| 1 00 06 * Write 1 00 07 * Write 1 00 08 * Write | X X X | Enable offline self test Enable online self test Disable self test | Disable |
| 1 00 10 Write | Vector word | Transmit vector word mode code | |
| 1 00 13 * Write | BIT word | Transmit BIT word mode code | |
| 1 01 n to Write 1 1E n | Data transmitted by RT | First data word Address = n-1 Last data word Address = 0 | |
| 1 1F 10 Write | Vector word | Transmit vector word mode code | |
| 1 1F 13 * Write | BIT word | Transmit BIT word mode code | |
| 2 00 11 Read | Synchronize word | Broadcast Synchronize with data mode code | |
| 2 01 n to Read 2 1E n | Broadcast data received by RT | First data word Address = n-1 Last data word Address = 0 | |
| 2 1F 11 Read | Synchronize word | Broadcast Synchronize with data mode code | |

*MSB of address (ADIN 11) = dont care (ie. 1 or 0)

BUS CONTROLLER

| Address | Data | Function / Comments | Reset |
|------------------------------------|---|--|-------|
| 0 00 00 * Read | Status received by BC | Read Status Memory | |
| 0 00 00 * Write 0 00 01 * Write | Command transmitted by BC First command for RT to RT | Initiate BC sequence Write before Command 0 00 00 | |
| 0 00 10 * Write 0 00 18 * Write | X X | Select bus 0 Select bus 1 | Bus 0 |
| 0 00 11 Write | Synchronize word | Synchronize with data mode code | |
| 0 00 12 Read | Error contents | Valid when ERROR | |
| 0 00 14 Write | 0000 0001 | Selected transmitter shutdown (bus 0) Selected transmitter shutdown (bus 1) | |

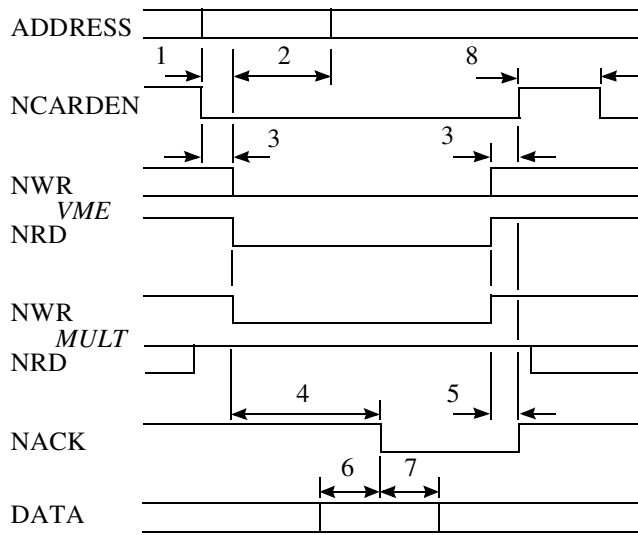
BUS CONTROLLER con't

| Address | Data | Function / Comments | Reset |
|--|-------------------------------------|--|---------|
| 0 00 15 Write | 0000 0001 | Override selected transmitter shutdown (bus 0) Override selected transmitter shutdown (bus 1) | |
| 0 01 n to Write 0 1E n | Data transmitted by BC | First data word Address = n-1 Last data word Address = 0 | |
| 0 1F 11 Write | Synchronize word | Synchronize with data mode code | |
| 0 1F 14 Write | 0000 0001 | Selected transmitter shutdown (bus 0) Selected transmitter shutdown (bus 1) | |
| 0 1F 15 Write | 0000 0001 | Override selected transmitter shutdown (bus 0) Override selected transmitter shutdown (bus 1) | |
| 1 00 00 Write 1 00 01 Write | X X | Select RT Select BC | RT |
| 1 00 02 * Write 1 00 03 * Write 1 00 04 * Write 1 00 05 * Write | X X X X | Disable BTL write Disable BTL read Enable BTL write Disable BTL read Disable BTL write Enable BTL read Enable BTL write Enable BTL read | Enable |
| 1 00 06 * Write 1 00 07 * Write 1 00 08 * Write | X X X | Enable offline self test Enable online self test Disable self test | Disable |
| 1 00 10 Read | Vector word | Transmit vector word mode code | |
| 1 00 12 Read | Last command word | Transmit last command word mode code | |
| 1 00 13 Read | BIT word | Transmit BIT word mode code | |
| 1 01 n to Read 1 1E n | Data received by BC | First data word Address = n-1 Last data word Address = 0 | |
| 1 1F 10 Read | Vector word | Transmit vector word mode code | |
| 1 1F 12 Read | Last command word | Transmit last command word mode code | |
| 1 1F 13 Read | BIT word | Transmit BIT word mode code | |
| 2 00 11 Write | Synchronize word | Broadcast synchronize with data mode code | |
| 2 00 14 Write | 0000 0001 | Bcast selected transmitter shutdown (bus 0) Bcast selected transmitter shutdown (bus 1) | |
| 2 00 15 Write | 0000 0001 | Bcast override sel transmitter shutdown (bus 0) Bcast override sel transmitter shutdown (bus 1) | |
| 2 01 n to Write 2 1E n | Broadcast data transmitted by BC | First data word Address = n-1 Last data word Address = 0 | |
| 2 1F 11 Write | Synchronize word | Broadcast synchronize with data mode code | |
| 2 1F 14 Write | 0000 0001 | Bcast selected transmitter shutdown (bus 0) Bcast selected transmitter shutdown (bus 1) | |
| 2 1F 15 Write | 0000 0001 | Bcast override sel transmitter shutdown (bus 0) Bcast override sel transmitter shutdown (bus 1) | |

* MSB of address (ADIN 11) = dont care (ie. 1 or 0)

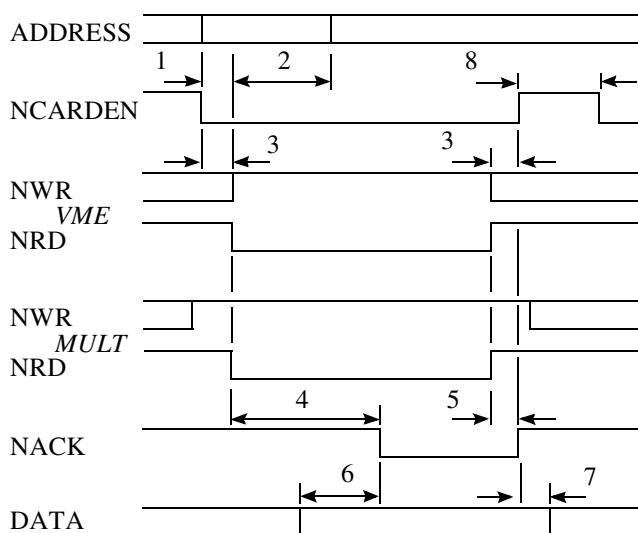
DETAILED TIMING

WRITE CYCLE



| | MIN | MAX | UNIT |
|--|------|------|------|
| 1. Set up time, address to write | 0 | | nS |
| 2. Hold time, write to address | 250 | | nS |
| 3. Set up and hold time NCARDEN to write | 0 | | nS |
| 4. Delay time write to NACK: | | | |
| Write to BTL RAM * | 250 | 450 | nS |
| Write to main RAM ** | 500 | 750 | nS |
| Write to 0 00 00 & 0 00 01 (BC) | 1000 | 1250 | nS |
| 5. Delay time write to NACK | 0 | 50 | nS |
| 6. Set up time data to NACK | 50 | | nS |
| 7. Hold time NACK to data | 50 | | nS |
| 8. Gap between writes | 20 | | nS |

READ CYCLE

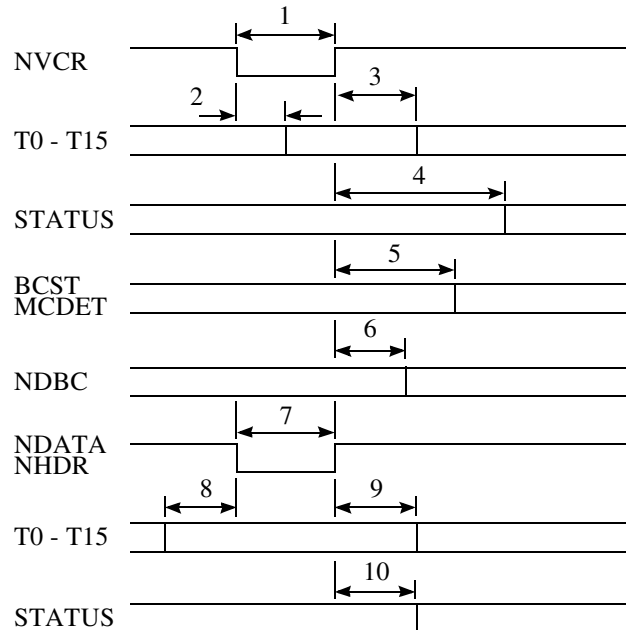


| | MIN | MAX | UNIT |
|---|--------------|-----|------|
| 1. Set up time, address to read | 0 | | nS |
| 2. Hold time, read to address | 250 | | nS |
| 3. Set up and hold time NCARDEN to read | 0 | | nS |
| 4. Delay time read to NACK: | | | |
| First read from BTL RAM ** | 500 + 250/wd | | nS |
| Subsequent read from BTL RAM | 250 | 450 | nS |
| Read from main RAM ** | 500 | 750 | nS |
| 5. Delay time read to NACK | 0 | 50 | nS |
| 6. Data available to NACK | 50 | | nS |
| 7. Data available after NACK | 0 | | nS |
| 8. Gap between reads | 130 | | nS |

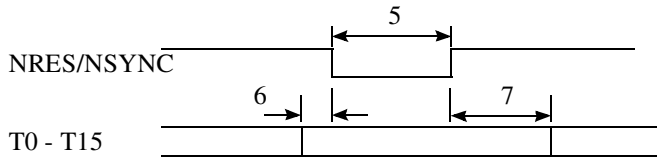
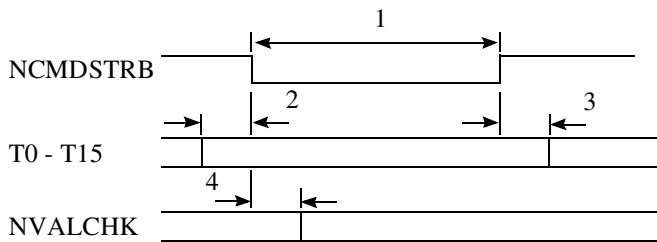
*After the last word is written to the BTL RAM, the contents of this RAM are transferred to the main RAM. Access to the BTL or main RAM is locked out during this time by delaying NACK. This transfer takes 500 nS + 250 nS/word.

**If the 1553 terminal is busy transferring data to or from the main RAM, access to this RAM is locked out until the transfers are complete by delaying NACK. These transfers take 8.5 μS + 1 μS/word (transmit) or 500 nS/word (receive).

DISCRETE SIGNALS (RT)

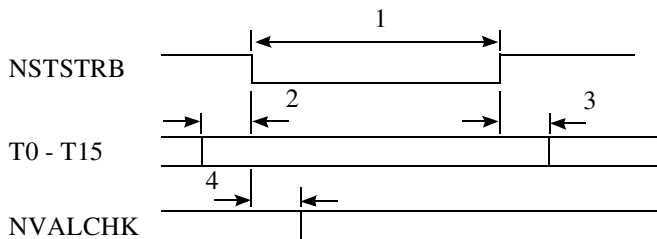


| | MIN | MAX | UNIT |
|--|-----|-----|------|
| 1. NVCR pulse duration | 500 | 650 | nS |
| 2. NVCR to T0-T15 valid | | 250 | nS |
| 3. NVCR to T0-T15 invalid | 250 | | nS |
| 4. NVCR to discrete status inputs (not rec) | | 600 | nS |
| 5. NVCR to BCST & MCDET valid | | 400 | nS |
| 6. NVCR to NDBC valid | | 200 | nS |
| 7. NDATA & NHDR pulse duration | 475 | 525 | nS |
| 8. T0-T15 valid to NDATA & NHDR | 250 | | nS |
| 9. NDATA & NHDR to T0-T15 invalid | 250 | | nS |
| 10. Last NDATA to discrete status inputs (rec) | | 250 | nS |



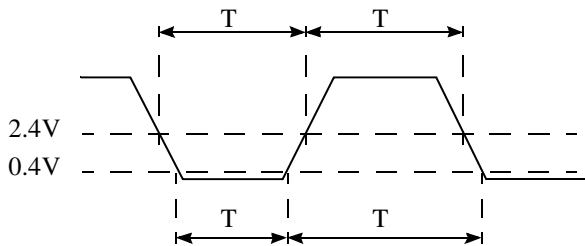
| | MIN | MAX | UNIT |
|---------------------------------|------|------|------|
| 1. NCMDSTRB duration | 8475 | 8525 | nS |
| 2. T0-T15 valid to NCMDSTRB | 100 | | nS |
| 3. NCMDSTRB to T0-T15 invalid | 100 | | nS |
| 4. NCMDSTRB to NVALCHK valid | | 100 | nS |
| 5. NRES/NSYNC pulse duration | 475 | 525 | nS |
| 6. T0-T15 valid to NSYNC | 50 | | nS |
| 7. NSYNC to T0-T15 invalid | 250 | | nS |
| 8. NVCR to NCMDSTRB (trans) | 7.8 | 8.8 | uS |
| Last NDATA to NCMDSTRB (rec) | 8.1 | 9.1 | uS |
| 9. NVCR to NRES/NSYNC non bcast | 27.9 | 28.1 | uS |
| NVCR to NRES/NSYNC bcast | 8.9 | 9.1 | uS |

DISCRETE SIGNALS (BC)



| | MIN | MAX | UNIT |
|------------------------------|------|------|------|
| 1. NSTSTRB duration | 8475 | 8525 | nS |
| 2. T0-T15 valid to NSTSTRB | 100 | | nS |
| 3. NSTSTRB to T0-T15 invalid | 100 | | nS |
| 4. NSTSTRB to NVALCHK valid | | 100 | nS |

16 MHZ CLOCK REQUIREMENT

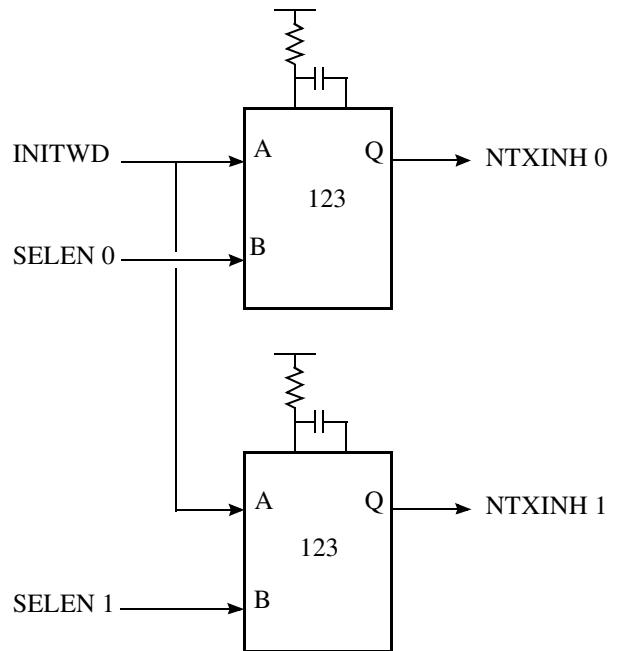


| T | MIN | MAX | of cycle |
|---|-----|-----|----------|
| | 40% | 60% | |

WATCHDOG TIMERS

There are two levels of failsafe timers within the device.

1. Counters to prohibit more than 32 data words being transmitted.
2. Timers to terminate transmission longer than 800 μ S. If additional external failsafe timers are required they may be connected as follows:-

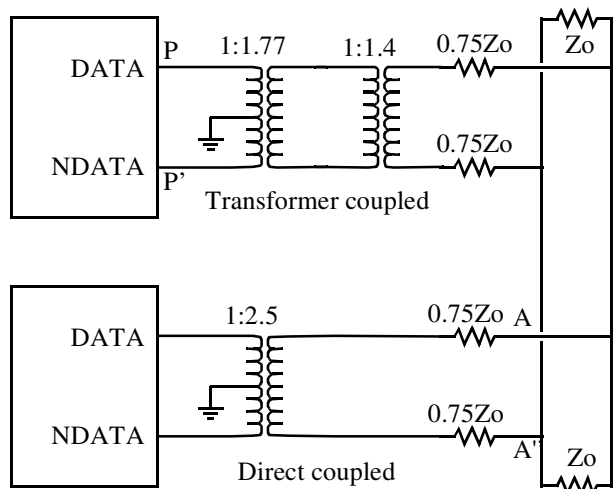


TRANSFORMERS

The device requires a 1:2.5 turns ratio for direct coupling and 1:1.77 turns ratio for transformer coupling. The center tap of the transformers must be tied to ground.

The suggested transformer is:

Technitrol 1553-35,45



OPERATING CONDITIONS

ABSOLUTE MAXIMUM RATINGS

| | | |
|--|----------------------|-------|
| V _{DD} Supply voltage | +7 | Volts |
| V _{SS} Supply voltage | 0 | Volts |
| V _{IH} High level input voltage | V _{DD} +0.5 | Volts |
| V _{IL} Low level input voltage | V _{SS} -0.5 | Volts |
| Operating free air temperature range | Per Configuration | |
| Storage temperature range | -65 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

| | MIN | NOM | MAX | UNIT |
|--------------------------------|------|-----|------|-------|
| V _{DD} Supply voltage | 4.75 | 5.0 | 5.5 | Volts |
| Free air temperature range | -55 | | +125 | °C |

ELECTRICAL CHARACTERISTICS

DIGITAL SIGNALS

MIN NOM MAX UNIT

A1. INPUT WITH PULL UP

| | | | | |
|--|-----------------|----|-----|-------|
| V _{IH} High level input voltage | 2.4 | | oc | Volts |
| V _{IL} Low level input voltage | V _{SS} | | 0.8 | Volts |
| I _{IH} High level input current | | | 10 | uA |
| I _{IL} Low level input current | 35 | 65 | 120 | uA |
| C _{IN} Input capacitance | | | 10 | pf |

A2. INPUT WITH PULL UP

| | | | | |
|--|-----------------|-----|------|-------|
| V _{IH} High level input voltage | 2.4 | | oc | Volts |
| V _{IL} Low level input voltage | V _{SS} | | 0.8 | Volts |
| I _{IH} High level input current | | | 10 | uA |
| I _{IL} Low level input current | 450 | 800 | 1500 | uA |
| C _{IN} Input capacitance | | | 10 | pf |

B. INPUT WITH PULL DOWN

| | | | | |
|--|-----|----|-----------------|-------|
| V _{IH} High level input voltage | 2.4 | | V _{DD} | Volts |
| V _{IL} Low level input voltage | oc | | 0.8 | Volts |
| I _{IH} High level input current | 35 | 65 | 120 | uA |
| I _{IL} Low level input current | | | 10 | uA |
| C _{IN} Input capacitance | | | 10 | pf |

C. OUTPUT

| | | | | |
|---|----------------------|-----|-----------------|-------|
| V _{OH} High level output voltage | V _{DD} -0.5 | | V _{DD} | Volts |
| V _{OL} Low level output voltage | | | 0.4 | Volts |
| I _{OH} High level output current | 2.0 | 5.5 | 10.0 | mA |
| I _{OL} Low level output current | 2.0 | 5.5 | 10.0 | mA |

D. OPEN DRAIN OUTPUT

| | | | | |
|---|-----|-----|------|-------|
| V _{OH} High level output voltage | | | oc | Volts |
| V _{OL} Low level output voltage | | | 0.4 | Volts |
| I _{OH} High level output current | | | 10 | uA |
| I _{OL} Low level output current | 2.0 | 5.5 | 10.0 | mA |

MIN NOM MAX UNIT

E. TRISTATE OUTPUT

| | | | | |
|---|----------------------|-----|-----------------|-------|
| V _{OH} High level output voltage | V _{DD} -0.5 | | V _{DD} | Volts |
| V _{OL} Low level output voltage | | | 0.4 | Volts |
| I _{OH} High level output current | 2.0 | 5.5 | 10.0 | mA |
| I _{OL} Low level output current | 2.0 | 5.5 | 10.0 | mA |
| I _{HZ} High impedance IO current | | | 10 | uA |

F. INPUT OUTPUT

| | | | | |
|---|----------------------|-----|-----------------|-------|
| V _{IH} High level input voltage | 2.4 | | V _{DD} | Volts |
| V _{IL} Low level input voltage | V _{SS} | | 0.8 | Volts |
| I _{IH} High level input current | | | 10 | uA |
| I _{IL} Low level input current | | | 10 | uA |
| C _{IN} Input capacitance | | | 10 | pf |
| V _{OH} High level output voltage | V _{DD} -0.5 | | V _{DD} | Volts |
| V _{OL} Low level output voltage | | | 0.4 | Volts |
| I _{OH} High level output current | 2.0 | 5.5 | 10.0 | mA |
| I _{OL} Low level output current | 2.0 | 5.5 | 10.0 | mA |
| I _{HZ} High impedance IO current | | | 10 | uA |

G. INPUT OUTPUT WITH PULL UP

| | | | | |
|---|----------------------|-----|-----------------|-------|
| V _{IH} High level input voltage | oc | | oc | Volts |
| V _{IL} Low level input voltage | V _{SS} | | 0.8 | Volts |
| I _{IH} High level input current | | | 10 | uA |
| I _{IL} Low level input current | 450 | 800 | 1500 | uA |
| C _{IN} Input capacitance | | | 10 | pf |
| V _{OH} High level output voltage | V _{DD} -0.5 | | V _{DD} | Volts |
| V _{OL} Low level output voltage | | | 0.4 | Volts |
| I _{OH} High level output current | 0.5 | 1.0 | 1.8 | mA |
| I _{OL} Low level output current | 1.5 | 5.0 | 9.0 | mA |

DATA BUS SIGNALS

H. TRANSMITTER

| | | | | |
|---|-----|-----|----------|-------------------|
| I _O Driver peak output current (CT2577) | | | 600 | mA |
| | | | (CT2579) | 750 |
| V _O Differential output level | 6.0 | 7.5 | 9.0 | V _{p-p} |
| point A-A' (R _L =35 ohms) | | | | |
| T _{RF} Rise / Fall times (CT2577) | 100 | 200 | 300 | nS |
| (10%-90% of p-p output) | | | | |
| T _{RF} Rise / Fall times (CT2579) | 200 | | 300 | nS |
| (10%-90% of p-p output) | | | | |
| V _{OS} Output offset 2.5 μS after mid bit crossing of parity, point A-A' (R _L =35 ohms) | | | 90 | mV _{p-p} |

H. RECEIVER

| | | | | |
|---|------|------|------|------------------|
| V _{IDR} Differential input level | | 14 | 20 | V _{p-p} |
| point P-P' | | | | |
| CMRR Common mode rejection ratio | 45 | | | dB |
| V _{TH} Input threshold voltage referred point A-A' (100KHz-1MHz) | 0.60 | 0.82 | 1.20 | V _{p-p} |

PIN ASSIGNMENTS - PGA PACKAGE

| # | PIN No | Signal | IO Type | # | PIN No | Signal | IO Type |
|----|--------|------------|---------|-----|--------|------------|---------|
| 1 | A1 | VME | A1 | 61 | N13 | NEMPTY | C |
| 2 | C2 | INITWD | C | 62 | L12 | NDBCA | A2 |
| 3 | D3 | T 13 | E | 63 | K11 | NNEWBUS | A1 |
| 4 | B1 | ADIN 11 | A1 | 64 | M13 | NTXINH 0 | A1 |
| 5 | C1 | T 14 | E | 65 | L13 | NTXINH 1 | A1 |
| 6 | D2 | ADIN 10 | A1 | 66 | K12 | SELEN 1 | C |
| 7 | E3 | T 15 | E | 67 | J11 | DATA 0 | F |
| 8 | D1 | ADIN 9 | A1 | 68 | K13 | DATA 1 | F |
| 9 | E2 | BCNRT | C | 69 | J12 | NSSFLAG | A2 |
| 10 | E1 | NSYNC | C | 70 | J13 | UB | A1 |
| 11 | F3 | ADIN 8 | A1 | 71 | H11 | NBUSY | A2 |
| 12 | F2 | Reserved | - | 72 | H12 | Reserved | - |
| 13 | F1 | MCAIR | B | 73 | H13 | NBIT16 | B |
| 14 | G1 | NVALCHK | C | 74 | G13 | NHDR | C |
| 15 | G3 | STATUS | D | 75 | G11 | DATA 2 | F |
| 16 | G2 | ADIN 7 | A1 | 76 | G12 | STREL | C |
| 17 | H1 | ADIN 6 | A1 | 77 | F13 | DATA 3 | F |
| 18 | H2 | NENCHK | A1 | 78 | F12 | NSR | A2 |
| 19 | H3 | MCDET | C | 79 | F11 | DATA 4 | F |
| 20 | J1 | WATCHDOG | C | 80 | E13 | DATA 5 | F |
| 21 | J2 | NVCR | C | 81 | E12 | WRAPEN | B |
| 22 | K1 | BCST | C | 82 | D13 | DATA 6 | F |
| 23 | J3 | NTF | A2 | 83 | E11 | T 0 | E |
| 24 | K2 | ADIN 5 | A1 | 84 | D12 | DATA 7 | F |
| 25 | L1 | ADIN 4 | A1 | 85 | C13 | DATA 8 | F |
| 26 | L2 | NME | A2 | 86 | C12 | T 1 | E |
| 27 | K3 | ADDR E | A1 | 87 | D11 | T 2 | E |
| 28 | M1 | SELEN 0 | C | 88 | B13 | DATA 9 | F |
| 29 | M2 | NDBC | C | 89 | B12 | DATA 10 | F |
| 30 | L3 | EOT | C | 90 | C11 | DATA 11 | F |
| 31 | N1 | ADDR D | A1 | 91 | A13 | T 3 | E |
| 32 | M3 | ADDR C | A1 | 92 | B11 | T 4 | E |
| 33 | L4 | ADDR B | A1 | 93 | C10 | T 5 | E |
| 34 | N2 | NWR | A1 | 94 | A12 | DATA 12 | F |
| 35 | N3 | ADDR A | A1 | 95 | A11 | T 6 | E |
| 36 | M4 | NRD | A1 | 96 | B10 | DATA 13 | F |
| 37 | L5 | NACK | D | 97 | C9 | DATA 14 | F |
| 38 | N4 | ADDR P | A1 | 98 | A10 | T 7 | E |
| 39 | M5 | Reserved | - | 99 | B9 | Reserved | - |
| 40 | N5 | DATABUS 0 | H | 100 | A9 | DATABUS 1 | H |
| 41 | L6 | NDATABUS 0 | H | 101 | C8 | NDATABUS 1 | H |
| 42 | M6 | NSTSTRB | C | 102 | B8 | NFULL | C |
| 43 | N6 | NCARDEN | A1 | 103 | A8 | DATA 15 | F |
| 44 | N7 | ERROR | C | 104 | A7 | NENBTL | A1 |
| 45 | L7 | VDD | - | 105 | C7 | VDD | - |
| 46 | M7 | VSS | - | 106 | B7 | VSS | - |
| 47 | N8 | Reserved | - | 107 | A6 | Reserved | - |
| 48 | M8 | INHMC | B | 108 | B6 | Reserved | - |
| 49 | L8 | NINHST | A1 | 109 | C6 | NILLCMD | A2 |
| 50 | N9 | C16MHZ | A2 | 110 | A5 | Reserved | - |
| 51 | M9 | LA | A1 | 111 | B5 | Reserved | - |
| 52 | N10 | NDATA | C | 112 | A4 | T 8 | E |
| 53 | L9 | ADIN 3 | A1 | 113 | C5 | Reserved | - |
| 54 | M10 | ADIN 2 | A1 | 114 | B4 | Reserved | - |
| 55 | N11 | ADIN 1 | A1 | 115 | A3 | T 9 | E |
| 56 | M11 | NRES | G | 116 | B3 | Reserved | - |
| 57 | L10 | ADIN 0 | A1 | 117 | C4 | T 10 | E |
| 58 | N12 | Reserved | - | 118 | A2 | T 11 | E |
| 59 | M12 | Reserved | - | 119 | B2 | T 12 | E |
| 60 | L11 | NCMDSTRB | C | | | | |

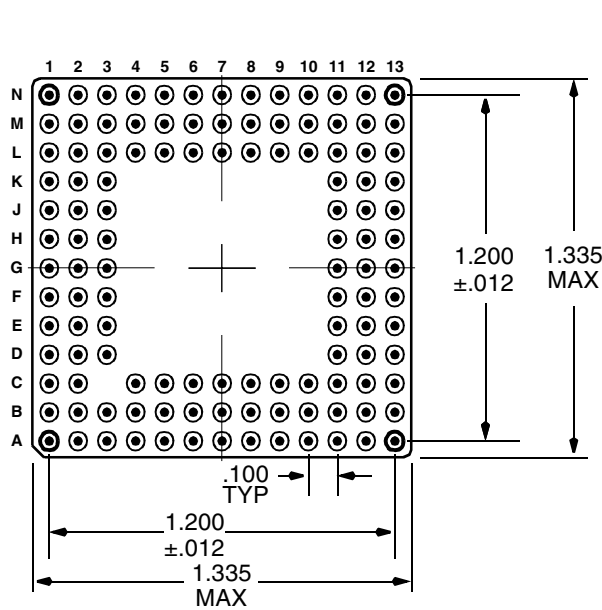
PIN ASSIGNMENTS - FLAT PACKAGE

| PIN No | Signal | IO Type | PIN No | Signal | IO Type |
|--------|---------------|---------|--------|---------------|---------|
| 1 | ADIN 11 | A1 | 43 | NCMDSTRB | C |
| 2 | ADIN 10 | A1 | 44 | NEMPTY | C |
| 3 | ADIN 09 | A1 | 45 | DATA 00 | F |
| 4 | BCNRT | C | 46 | DATA 01 | F |
| 5 | NSYNC | C | 47 | NSSFLAG | A2 |
| 6 | ADIN 08 | A1 | 48 | UB | A1 |
| 7 | Not Connected | - | 49 | NBIT16 | B |
| 8 | Not Connected | - | 50 | Not Connected | - |
| 9 | ADIN 07 | A1 | 51 | DATA 02 | F |
| 10 | ADIN 06 | A1 | 52 | Not Connected | - |
| 11 | MCDET | C | 53 | DATA 03 | F |
| 12 | NVCR | C | 54 | DATA 04 | F |
| 13 | BCST | C | 55 | DATA 05 | F |
| 14 | NTF | A2 | 56 | WRAPEN | B |
| 15 | ADIN 05 | A1 | 57 | DATA 06 | F |
| 16 | ADIN 04 | A1 | 58 | T 00 | E |
| 17 | NME | A2 | 59 | DATA 07 | F |
| 18 | ADDR E | A1 | 60 | DATA 08 | F |
| 19 | NDBC | C | 61 | T 01 | E |
| 20 | EOT | C | 62 | T 02 | E |
| 21 | ADDR D | A1 | 63 | DATA 09 | F |
| 22 | ADDR C | A1 | 64 | TA 10 | - |
| 23 | ADDR B | A1 | 65 | DATA 11 | F |
| 24 | NWR | A1 | 66 | T 03 | E |
| 25 | ADDR A | A1 | 67 | T 04 | E |
| 26 | NRD | A1 | 68 | T 05 | E |
| 27 | NACK | D | 69 | DATA 12 | F |
| 28 | ADDR P | A1 | 70 | T 06 | E |
| 29 | DATA (Bus 0) | H | 71 | DATA 13 | F |
| 30 | NDATA (Bus 0) | H | 72 | DATA 14 | F |
| 31 | NSTSTRB | C | 73 | T 07 | E |
| 32 | NCARDEN | A1 | 74 | DATA (Bus 1) | - |
| 33 | ERROR | C | 75 | NDATA (Bus1) | - |
| 34 | VDD1 | - | 76 | NFULL | C |
| 35 | VSS1 | - | 77 | DATA 15 | F |
| 36 | C16MHZ | A2 | 78 | VDD2 | - |
| 37 | LA | A1 | 79 | VSS2 | - |
| 38 | ADIN 03 | A1 | 80 | NILLCMD | A2 |
| 39 | ADIN 02 | A1 | 81 | T 08 | E |
| 40 | ADIN 01 | A1 | 82 | T 09 | E |
| 41 | NRES | G | 83 | T 10 | E |
| 42 | ADIN 00 | A1 | 84 | VME / MULTI* | A1 |

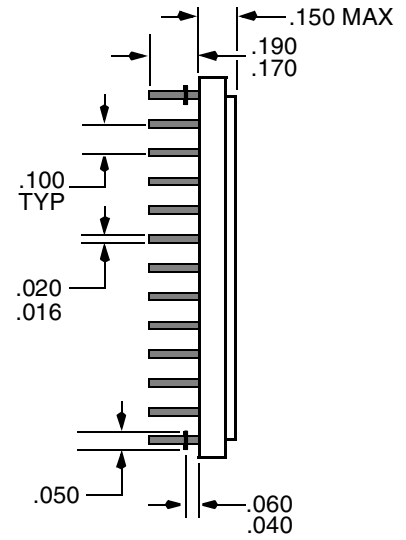
PACKAGE OUTLINE

Plug In – 119 Pin PGA

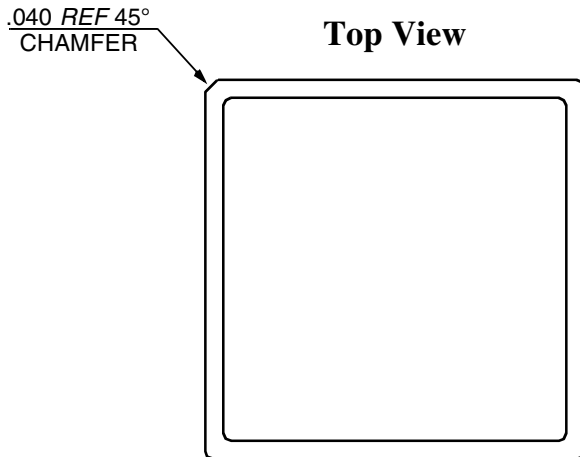
Bottom View



Side View



Top View



POWER SUPPLY REQUIREMENTS

CURRENT

- Transmitter standby (both channels)
- 50% duty cycle (one channel)
- 100% duty cycle (one channel)

| MAX | UNIT |
|-----|------|
| 60 | mA |
| 350 | mA |
| 650 | mA |

POWER DISSIPATION

- Transmitter standby (both channels)
- 50% duty cycle (one channel)
- 100% duty cycle (one channel)

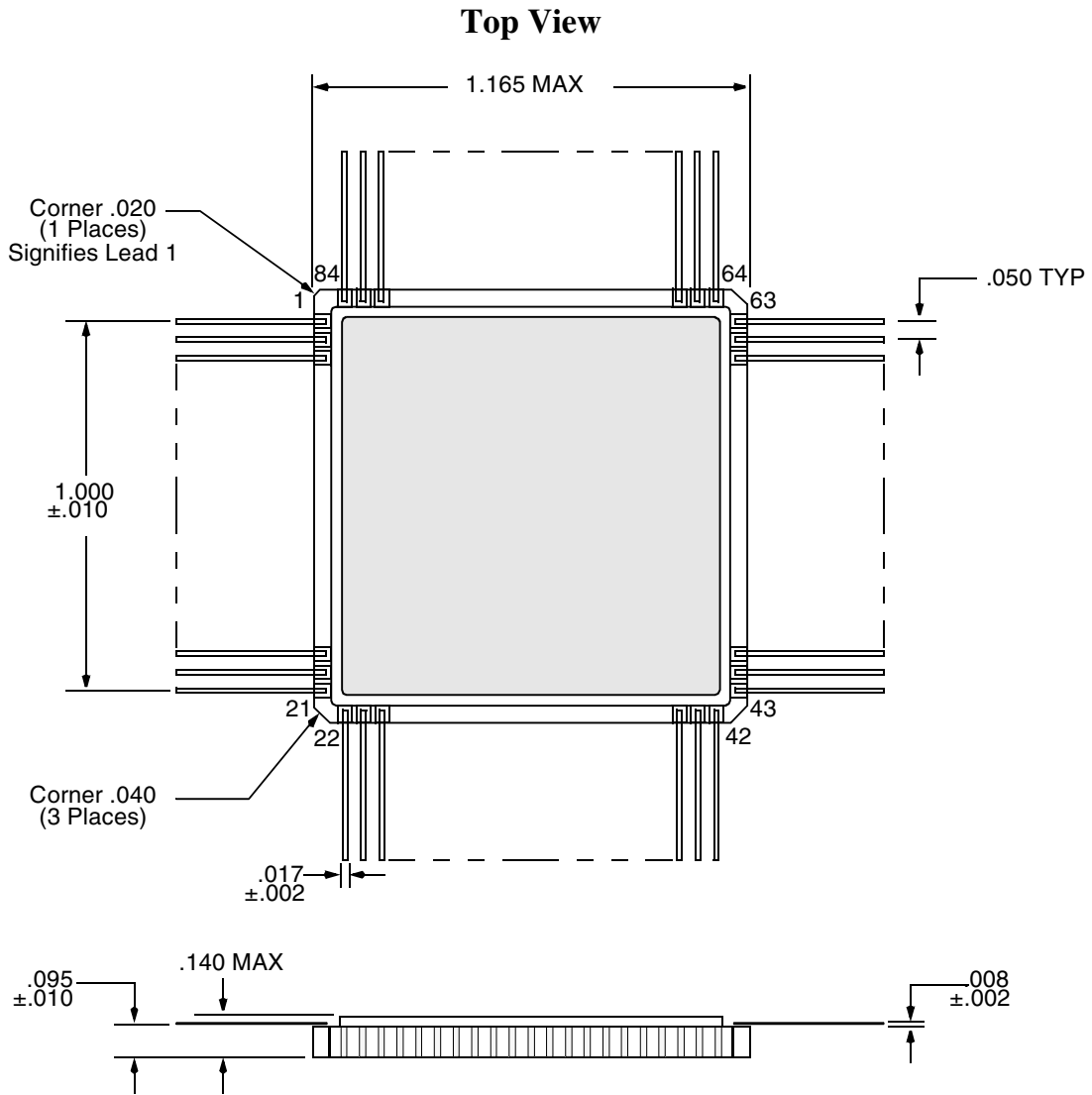
| MAX | UNIT |
|-----|-------|
| 0.3 | watts |
| 0.6 | watts |
| 0.9 | watts |

POWER SUPPLY DECOUPLING

To maximise stabilization of the devices transceivers, a 4.7 uf and a 0.1 uf capacitor should be connected in parallel from the +5V supply to ground.

PACKAGE OUTLINE

Flat Package – 84 Leads CQFP



ORDERING INFORMATION

| Model Number * | T-BUS Width | MIL-STD-1760 Pinout | McAir Compliant | DESC Part Number | Package | | |
|-------------------|-------------|---------------------|-----------------|------------------|-------------|-----|--------------|
| CT2577-10-QM-P119 | T0-T15 | ✓ | | TBD | 119 Pin PGA | | |
| CT2577-10-XT-P119 | | ✓ | | | | | |
| CT2577-10-IN-P119 | | ✓ | | | | | |
| CT2577-10-CG-P119 | | ✓ | | | | | |
| CT2577-01-QM-F84 | T0-T10 | | | | | | 84 Lead CQFP |
| CT2577-01-XT-F84 | | | | | | | |
| CT2577-01-IN-F84 | | | | | | | |
| CT2577-01-CG-F84 | | | | | | | |
| CT2577-11-QM-F84 | | ✓ | | | | | |
| CT2577-11-XT-F84 | | ✓ | | | | | |
| CT2577-11-IN-F84 | | ✓ | | | | | |
| CT2577-11-CG-F84 | | ✓ | | | | | |
| CT2579-10-QM-P119 | T0-T15 | | | | ✓ | TBD | 119 Pin PGA |
| CT2579-10-XT-P119 | | | | | ✓ | | |
| CT2579-10-IN-P119 | | | | | ✓ | | |
| CT2579-10-CG-P119 | | | | | ✓ | | |
| CT2579-01-QM-F84 | T0-T10 | | ✓ | | | | 84 Lead CQFP |
| CT2579-01-XT-F84 | | | ✓ | | | | |
| CT2579-01-IN-F84 | | | ✓ | | | | |
| CT2579-01-CG-F84 | | | ✓ | | | | |
| CT2579-11-QM-F84 | | | ✓ | | | | |
| CT2579-11-XT-F84 | | | ✓ | | | | |
| CT2579-11-IN-F84 | | | ✓ | | | | |
| CT2579-11-CG-F84 | | | ✓ | | | | |

*** Screening Code Breakdown**

QM = MIL-STD-883 Compliant
 XT = Extended Temperature Range (-55°C to +125°C)
 IN = Industrial Temperature Range (-40°C to +85°C)
 CG = Commercial Temperature Range (-0°C to +70°C)

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