

RAD_{PAL} POWER-ON-RESET PERFORMANCE AT COLD TEMPERATURES

11/3/97

Power-On-Reset

UTMC's RAD_{PAL} device is designed to reset all of the I/O registers on power up. A functional limitation has been observed in the product relating to the Power-On-Reset circuit at cold temperatures. At cold temperature, V_{DD} must rise to a voltage greater than the minimum operating voltage of 4.5 volts before an internally generated power-on-reset (POR) signal goes inactive. The POR signal resets the RAD_{PAL}'s ten (10) internal macro-cell flip-flops.

Circuit Operation

The POR circuit schematic is shown in Figure 1. Transistors N1 and N2 operate as diodes with a forward voltage of typically 0.8 volts. P1 acts as a linear resistor to set a small bias current through N1 and N2. As V_{DD} rises from zero volts, the voltage at node A follows V_{DD} up to about 1.6 volts where it is clamped and rises only a few tenths of a volt higher as V_{DD} continues to rise to 5 volts.

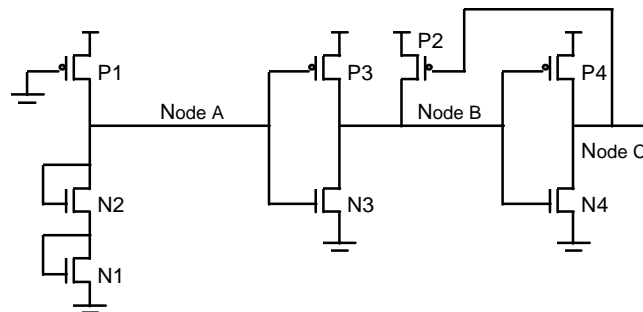


Figure 1.

The remaining transistors in Figure 1 configure a Schmitt trigger circuit, i.e., a non-inverting buffer with hysteresis. Node C is the POR signal that goes to the asynchronous reset input of a flip-flop. The switch point of inverters N3/P3 and N4/P4 is set by a switch point ratio factor multiplied by V_{DD} and is typically $0.4 \cdot V_{DD}$. As a result, Node A will initially look like a logic '1' to inverter N3/P3 as V_{DD} begins to rise. During that time node B will be logic '0' and node C will be logic '1' and transistor P2 is off. When V_{DD} rises to 4 volts, the switch point of inverter N3/P3 rises to a value above Node A voltage causing node A to appear as a logic '0'. Node B begins to rise and node C begins to fall. As node C falls, transistor P2 turns on and helps node B rise faster. The feedback provided by P2 causes the buffer to have very high gain and node C switches to '0' quickly. The purpose of P2 is to add hysteresis to the buffer so the switch point of N3/P3 will be higher and V_{DD} will have to drop lower before the reset becomes active again. A simulation with typical process parameters and room temperature is attached. Once the POR circuit switches, V_{DD} can drop below 4.5V before the POR asserts again resetting the macro-cell flip-flops.

The V_{DD} voltage at which the POR signal (node C) is removed is, defined by the voltage at which the switch point of inverter N3/P3 is equal to the reference voltage at node A. *If the reference*

voltage increases or if the switch point ratio decreases, V_{DD} must go higher before POR goes inactive.

The voltage at node A depends primarily on the N-channel threshold voltage. The switch point of the buffer depends on the ratio of N-channel to P-channel I_{DS} currents. Both of these depend on several circuit, process and environmental parameters including:

- transistor sizes
- oxide thickness
- transistor gate poly CD's (channel length)
- substrate and well doping
- mobility
- radiation
- temperature

These parameters cause the POR trigger point to vary over a wide range. According to worst case simulations, POR goes inactive anywhere between a V_{DD} voltage of 2.4 and 4.4 volts, nominally about 3.4 volts.

POR Circuit Limitation

At cold temperatures product evaluation shows that the POR signal remains active when V_{DD} is greater than 4.5 volts. This is due to the following circuit action.

N-channel thresholds are the most critical process parameter to the POR circuit. N-channel transistor thresholds increase at cold temperature. Consequently, the reference voltage at node A of Figure 1 increases, requiring V_{DD} to go higher than the nominal voltage of 3.4 volts before the switch point of N3/P3 exceeds the voltage level of Node A. The effect of a change in N-channel transistor thresholds on the V_{DD} level required to release POR is multiplied by a factor of four. For example, if the N-channel voltage threshold rises 180 mV from room temperature to -55°C, V_{DD} must rise 720mV volts higher than it would at room temperature before the POR signal is released. In addition to temperature variations, the N-channel voltage threshold is affected by process variations.

Another minor factor is that the total chip current increases at low temperature. This causes additional I-R drop in the V_{DD} and V_{SS} power busses. Therefore, the actual voltage across the POR circuit is less than the externally applied V_{DD} . Internal measurements on the bus showed the voltage varied about 30mV.

A positive voltage overshoot greater than 10ns in duration on V_{DD} will cause the POR to switch low. Because the voltage gain of the Schmitt trigger circuit is high and switches quickly, a short duration overshoot on V_{DD} is sufficient to cause the circuit to switch and remove the POR signal. Testing shows that the greater the number of I/O registers that are enabled by the RADPAL program code, the greater the value of V_{DD} required to remove the reset signal.

Characterization Data

A plot of temperature versus V_{DD} is attached. Note that the worst devices at -55°C can switch when V_{DD} is as high as 5.1 volts. If the minimum temperature is limited to about -15°C and the minimum V_{DD} is 4.75 volts, the POR will reset the internal flip-flops with a 99% confidence interval. The sample size for this data is 44 units.

Radiation Effect

Radiation causes N-channel thresholds to decrease which lowers the voltage at node A. This helps the POR circuit and makes it work according to spec at all temperatures. A data plot of V_{DD} vs. Temperature with 1.0M rads(Si), 300K rads(Si), 100K rads(Si) total dose is attached.

Work-Around

For customers using the registered outputs, it is necessary to change the temperature and voltage start-up specification for the RADPAL to reflect the POR circuit's limitation. Additionally, the application of voltages on the V_{DD} pin(s) of the RADPAL must start at 0V and reach 1V at a rate of 0.1V/s or faster. The power-up voltage on V_{DD} must be continuously increasing with respect to time, through 3V, and monotonic thereafter to V_{DD} minimum.

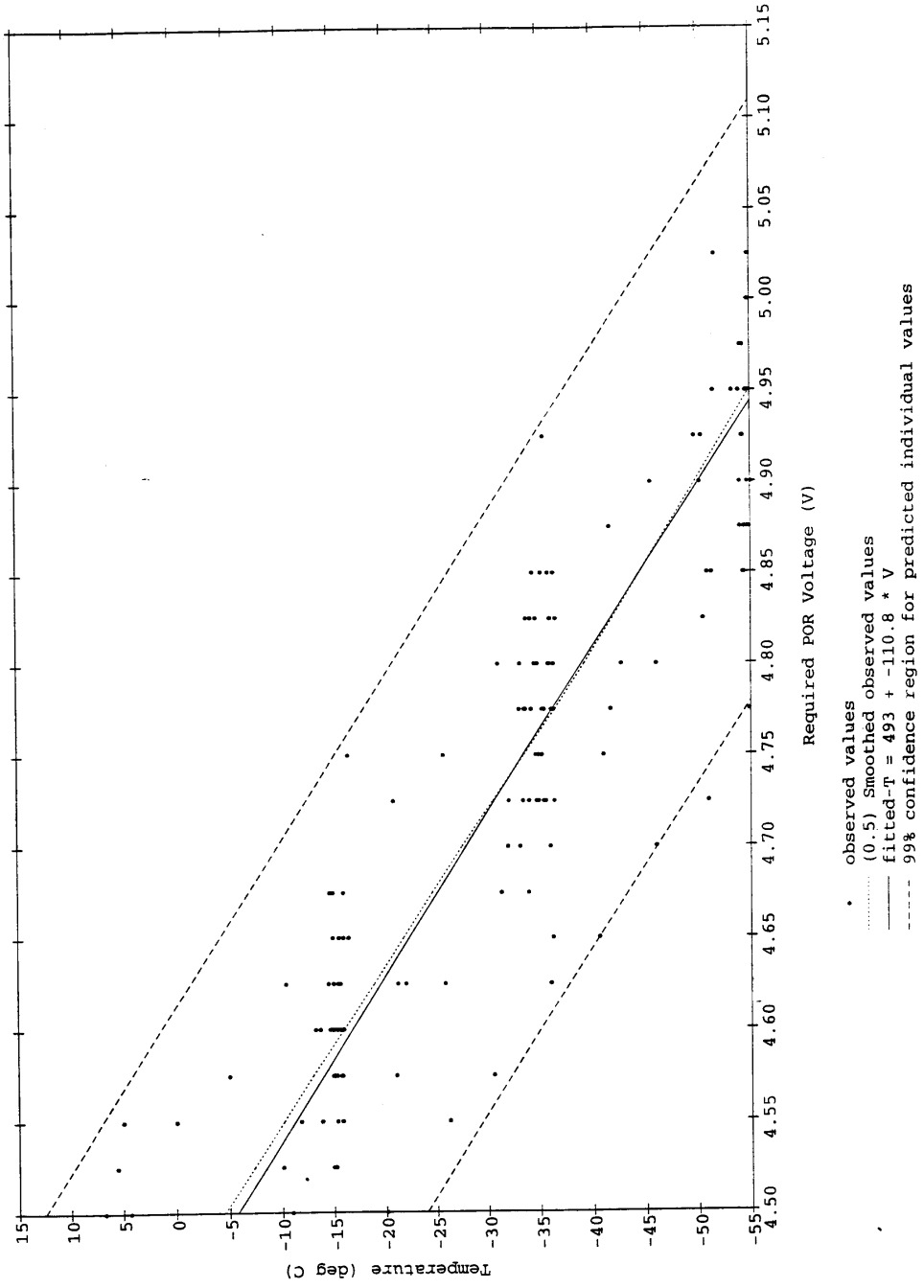
| Operating Temperature Range | Minimum V_{DD} for Start-Up |
|-----------------------------|-------------------------------|
| +125°C | 4.5V |
| +25°C | 4.5V |
| +12°C | 4.5V |
| -55°C | 5.1V |

Equation for minimum V_{DD} for Start-up from +12°C to -55°C

$$V_{DD} (\text{Min}) = -.0090*(^{\circ}\text{C}) + 4.61$$

Alternatively, a temperature range of -55°C to +125°C is possible if V_{DD} rises above 5.1 volts for more than 10ns on power-up. For additional operating points, use the equation above to determine the conditions that will work for a given system design.

UTMC PAL POR
Temperature vs Passing Voltage



UTMC PAL POR
Temperature vs Passing POR Voltage grouped by Radiation Dose
Sample size = 8

