

RADPAL POWER-ON-RESET VDD RAMP RATE REQUIREMENTS

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Introduction

It has been observed that the RADPAL has some limitations during power-up that are not covered in the original specification. The original specification simply requires VDD to rise monotonically. The purpose of this paper is to describe the updated requirements and specifications for the RADPAL power-up and the reason for the change.

Circuit Limitation

An anomaly was observed for a power-up application where a residual voltage between 200mV and 500mV was supplied to the VDD pin(s) of the RADPAL for several hundred milliseconds prior to the power supply ramping to 5 volts. As a result, the RADPAL enters a "test" mode (as opposed to a "user" mode). In the test mode, the output buffers are placed in a high impedance state and the RADPAL does not function as programmed.

Through HSPICE simulation and laboratory tests, UTMIC has found there exists a window in which a small residual voltage on the VDD pin(s) allows the RADPAL to power up in either the "user" mode or the "test" mode of operation. The anomaly is not seen when the application of power starts at zero volts and transitions monotonically to VDD minimum and the slew rate is greater than 0.1 volts/second. The anomaly is not wafer or lot dependent and affects all date codes.

Circuit Operation

After the RADPAL is programmed, the security fuse must be blown to ensure that the program code cannot be read and to ensure the RADPAL powers up in user mode. The attached schematic represents all the relevant circuitry to the power-up ramp limitation. Latch MD0 is the user mode latch and latch MD1 is a test mode latch. The TEST signal controls whether the part is in USER mode or TEST mode. The two tri-state inverters are enabled by MD1. If MD1 is low, a blown security fuse (low impedance) causes TSI-1 to pull node DAN high and TEST low which puts the part in user mode. If MD1 is high, TSI-2 is active and the security latch is enabled. The POR circuit is designed to reset the security latch on power-up, forcing TEST low and the part into user mode.

When TEST = '0', MD0 (user mode) is forced high and all test modes are forced inactive. The circuit is designed to power up in the user mode, if the security fuse is blown, regardless of the state of MD1 on power-up.

Circuit Analysis

A customer reported an intermittent problem during power-up where the RADPAL outputs were in a high impedance state which is not a condition the program code would cause. As a result, UTMIC engineers suspected the POR circuit in the security module was allowing the RADPAL to enter "test mode 1". It was found through testing and simulation that the POR signal did not

occur when the temperature was above 25C. This caused immediate concern and a detailed analysis of the problem was performed.

The analysis found that the RADPAL only failed if a residual voltage of about 400mV was on the VDD pin before power ramped to 5 volts. If VDD started at zero volts, the RADPAL always powered up correctly under all conditions of temperature, process parameters and VDD ramp rates. Yet, simulations and internal probing of the circuit showed the POR signal in the Security module did not always activate.

Simulation analysis of the entire chip brought to light that the circuit would always power up in user mode even if the POR signal failed to activate. This is because the state of the Security latch is determined during subthreshold operation before VDD reaches one volt. During subthreshold operation, both MD1 and the inverted MD1 signals that control the tri-state inverters are at a voltage level equal to approximately VDD/2. Thus, both TSI-1 and TSI-2 are enabled weakly. The security fuse provides a solid zero voltage to the input of TSI-1 which will try to pull node DAN high. Even when the POR signal does not rise above one volt, it always begins to rise during power up so that, during this initial sub-threshold region of operation, the voltage is sufficient to reset the latch with the help of TSI-1. This action causes node DAN to rise, keeping TEST at a logic zero. As VDD continues to rise, MD0 is forced high and MD1 is forced low which locks the chip into "user" mode. The RADPAL worked in simulations with worst case PAL wafer processing models, temperature ranging from -55C to +125C, and with VDD ramping 0 to 5 volts with a duration varying from 10 microseconds to 5 seconds.

Characterization Data

Attached is a table showing the data taken in the lab. The RADPAL passed under all the conditions shown. The circuit never failed to power up in user mode over all conditions of temperature and ramp rates as long as the initial VDD voltage was zero. The RADPAL is susceptible to powering up in a test mode whenever a residual voltage of between 200mV and 500mV is on the VDD pin prior to application of the 5 volt power supply.

Specifications

In order to avoid powering up the UT22VP10 RADPAL in a test mode, the following specifications must be met:

- 1) The application of voltages on the VDD pin of the RADPAL must start at zero volts and reach 1V at a rate of 0.1V/s or faster.
- 2) The power-up voltage must be continuously increasing with respect to time through 3V and monotonic thereafter.

An alternative or additional method to guarantee that the UT22VP10 RADPAL functions in the user mode of operation is to implement the following fix into the board level design:

- 1) Apply one of the opcodes shown in Table 1 to the corresponding inputs of the RADPAL. Notice that the Clock and I9 inputs must have a logic "1" applied during the application of a valid opcode.

Table 1: Valid Power-Up Opcodes

Mode of Operation	Power-Up Opcode (HEX) ¹	RAD _{PAL} Input Pins									
		I 9	I 8	I 7	I 6	I 5	I 4	I 3	I 2	I 1	Clk/I
0	DC	1	1	1	0	1	1	1	0	0	1
2	DE	1	1	1	0	1	1	1	1	0	1
3	DF	1	1	1	0	1	1	1	1	1	1
4	E0	1	1	1	1	0	0	0	0	0	1
5	E1	1	1	1	1	0	0	0	0	1	1
6	E2	1	1	1	1	0	0	0	1	0	1

Notes: 1. The Hexadecimal power-up opcode refers to the RADPAL inputs I8 - I1.

- Apply one of the opcodes from Table 1 for at least 100ns anytime after V_{DD} is within $5V \pm 10\%$ to ensure all test mode latches are cleared. Figure 1 shows the opcode timing diagram.

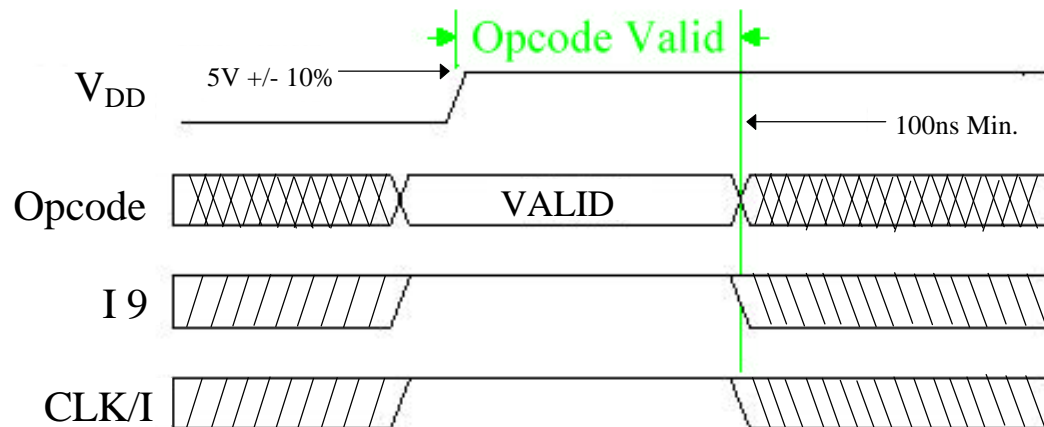


Figure 1. Opcode Timing

Applying one of the opcodes from Table 1 enables the programmed security fuse to reset the internal test latch, forcing the UT22VP10 RAD_{PAL} into the user mode of operation.

UT22VP10 RADPAL ^(TM)						
PART #	WAFER LOT	PART TYPE	TEMP.	RAMP FROM 0V to 5V	# OF CYCLES	FAILURES
87	QS52431	RC02A	125°C	300mS	1,189	0
69	QS52431	RC02A	125°C	300mS	1,720	0
16	QS48409	RC01A	125°C	300mS	1,002	0
2	QS20587	RC01A	125°C	300mS	1,015	0
3	QS20587	RC02A	125°C	300mS	1,008	0
4	QS20587	RC01A	125°C	300mS	2,102	0
87	QS52431	RC02A	25°C	300mS	53,466	0
87	QS52431	RC02A	90°C	300mS	15,344	0

RAMP FROM 0V to 5V (10 CYCLES PER PART, TEMPERATURE=25°C)													
PART#	100nS	200nS	500nS	1uS	10uS	50uS	100uS	200uS	500uS	1mS	10mS	50mS	100mS
87	P	P	P	P	P	P	P	P	P	P	P	P	P
69	P	P	P	P	P	P	P	P	P	P	P	P	P
16	P	P	P	P	P	P	P	P	P	P	P	P	P
2	P	P	P	P	P	P	P	P	P	P	P	P	P
3	P	P	P	P	P	P	P	P	P	P	P	P	P
4	P	P	P	P	P	P	P	P	P	P	P	P	P

P=PASS