

STEP-by-STEP Guide to 1553 Design

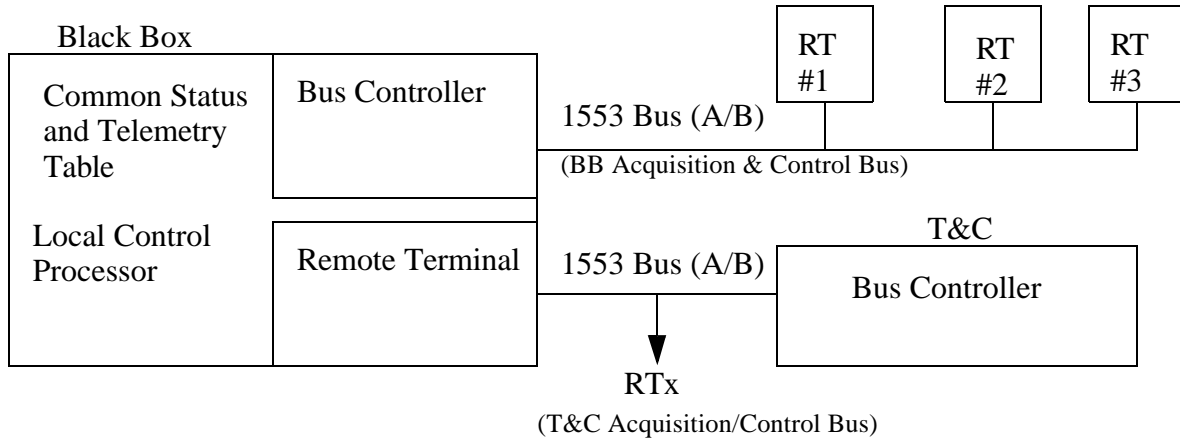
Preface

The purpose of this publication is to take a new 1553 designer through the basic steps required to complete a 1553 interface design. The designer will use a system specification and design a hardware implementation (including software routines). The example case begins with a high-level design specification for a black box. Given the 1553 aspects of the system specification the designer will assess the bus traffic verses local memory requirements, select the appropriate protocol device and design the interface. The example black box specification incorporates two of the three 1553 functions (Bus Controller and Remote Terminal).

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1.0 System Specification



1.1 Black Box Overview

The BB (black box) will be designed to accommodate a Bus Controller (BC) and Remote Terminal (RT) function. The BC and RT functions shall operate independently and in a stand-alone fashion. The Bus Controller will transmit the command lists outlined in section 4.2. A status and telemetry table will be maintained within the BC local memory and transmitted from the BB Remote Terminal to the T&C Bus Controller. The status and telemetry assignment and format is outlined in Table 1.

Table 1:

Bus Component	S/A#	Telemetry Item	BB Acq Rate	BBRT S/A	T&C Acq Rate
RT #1	3	Critical Sensor 1	200Hz	1	200Hz
	3	Critical Sensor 2	200Hz	1	200Hz
	2	Battery 1 Voltage	100Hz	1	200Hz
	2	Battery 2 Voltage	100Hz	1	200Hz
	2	Battery 1 Current	100Hz	1	200Hz
	2	Battery 2 Current	100Hz	1	200Hz

Table 1:

Bus Component	S/A#	Telemetry Item	BB Acq Rate	BBRT S/A	T&C Acq Rate
RT #2	3	Critical Sensor 3	200Hz	1	200Hz
	3	Critical Sensor 4	200Hz	1	200Hz
	2	ACS 1 Voltage	100Hz	1	200Hz
	2	ACS 1 Current	100Hz	1	200Hz
	2	Horizon Sensor 1	100Hz	1	200Hz
	2	Horizon Sensor 2	100Hz	1	200Hz
RT #3	3	Critical Sensor 5	200Hz	1	200Hz
	3	Critical Sensor 6	200Hz	1	200Hz
	2	Air Pressure AFT	100Hz	1	200Hz
	2	Air Pressure FRD	100Hz	1	200Hz
	2	Altimeter 1	100Hz	1	200Hz
	2	Altimeter 2	100Hz	1	200Hz

Within the system architecture the BB has the responsibility for short loop control function corrections. The BB maintains a table for the purpose of actuator control and feedback, which the T&C requests on a periodic basis. The outer control-loop is controlled by the T&C via a 1553 command sent to the position S/A for each RT. Inner-loop compensation is performed locally by the BB processor. Table 2 outlines the control and position information format.

Table 2:

Bus Component	S/A#	Actuator Item	BB CMD&Acq Rate	BBRT S/A	T&C Acq Rate	T&C CMD Rate
RT #2	1	Torque #1	400Hz	1	200Hz	
	1	Position #1	400Hz	1	200Hz	100Hz
	1	Torque #2	400Hz	1	200Hz	
	1	Position #2	400Hz	1	200Hz	100Hz
RT #3	1	Torque #3	400Hz	1	200Hz	
	1	Position #3	400Hz	1	200Hz	100Hz
	1	Torque #4	400Hz	1	200Hz	
	1	Position #4	400Hz	1	200Hz	100Hz

The BB sub-system status will be reported back to the T&C through the use of the SSF flag contained in the 1553 status response of the BB Remote Terminal; when the T&C controller receives this status response, a Transmit 1 data word command will be immediately issued to the BB Remote Terminal S/A 2. The BB Remote Terminal will respond with proper Status and the single data word. Refer to Appendix B for the BB Sub-system status word format (S/A 2). A periodic Synchronize Mode Code Command without data will be sent by the T&C Bus Controller, prior to the time-tag roll over; this Mode Code will synchronize the BB and the BB sub-system. All un-mentioned BB S/A's and MC's shall be illegalized during initialization.

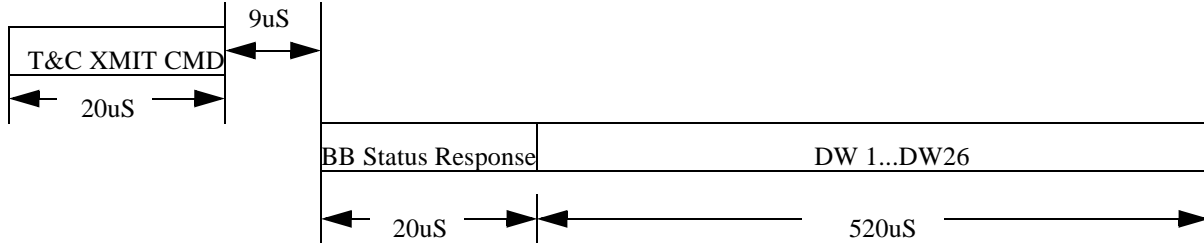
Based on the above system specification, evaluation regarding the BB architecture and design can be performed. The UT69R000 RISC micro-controller (R000) will be used as the core processor for the BB. Due to the operation of the system, the best telemetry and command solution will probably be the SμMMIT-DX; this architecture will allow the R000 to create and maintain a single table in local memory for the maintenance of all telemetry and command items. The use of a protocol device with on-board RAM would be slightly less effective since the processor would have to extract the telemetry and command items from the on-board memory and re-locate them into the processor's local memory.

2.0 Design Evaluation

Given the system parameters, calculate the 1553 and local memory bus requirements for each 1553 bus interface (RT and BC). For all examples, a 9uS response time will be used.

2.1 BB Remote Terminal

T&C sends a Transmit 26 Data Words Command to S/A #1 every 200Hz (1/5mS).

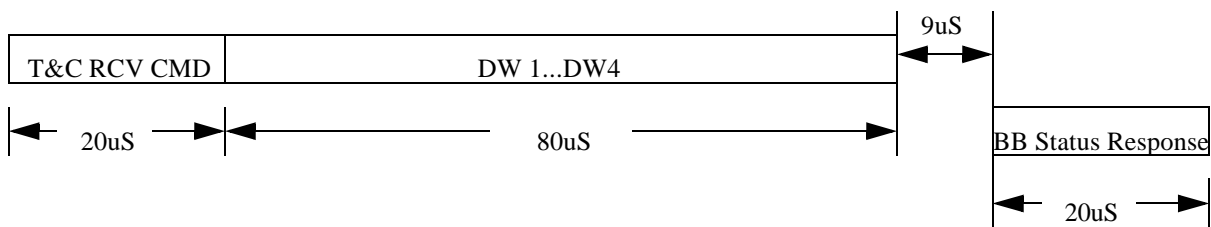


The duty cycle for the T&C 200Hz command is then expressed in terms of bus transmit time over the command repeat duration.

$$\frac{569\mu\text{S}}{5\text{ mS}} = 11.38\%$$

Next, consider the T&C command for actuator position.

The T&C sends a Receive 4 Data Words Command to S/A #1 every 100Hz (1/10mS) for actuator position control.



The duty cycle for the T&C 100Hz command is then expressed in terms of bus transmit time over the command repeat duration. Note the Σ MMIT bus usage percent is in terms of the 200Hz Frame; even though the 100Hz Frame occurs at half the rate of the 200Hz. This is due to the fact every second time through the 200Hz frame, the additional commands of the 100Hz are combined and sent with the 200Hz Frame commands. Therefore, to quantify a worst case 1553 bus usage vs. local bus, the total of the two should be examined, rather than a average based on the actual occurrence (one 100Hz command frame for every two 200Hz command frames).

Calculation of the total combined bus usage is as follows:

$$\frac{129\mu\text{S}}{10\text{ mS}} = 1.29\%$$

$$\begin{aligned}\text{Bus Usage} &= 11.38\% + 1.29\% \\ &= 12.67\%\end{aligned}$$

The BB RT local bus time required by the SμMMIT versus the 1553 message time is as follows:

$$\frac{333.36\text{nS (Descriptor Read)} + 2.167\mu\text{S (Read 26 Data Words)} + 500.04\text{nS (Descriptor Update)} + 166.7\text{nS (Interrupt log)}}{5\text{mS (200 Hz cycle time)}}$$

$$\frac{333.36\text{nS (Descriptor Read)} + 333.36\text{nS (Read 4 Data Words)} + 500.04\text{nS (Descriptor Update)} + 166.7\text{nS (Interrupt log)}}{10\text{mS (100 Hz cycle time)}}$$

$$\frac{\text{S}\mu\text{MMIT Bus Usage}}{\text{Frame Cycle Time}} = \frac{4.5\mu\text{S}}{5.0\text{mS}}$$

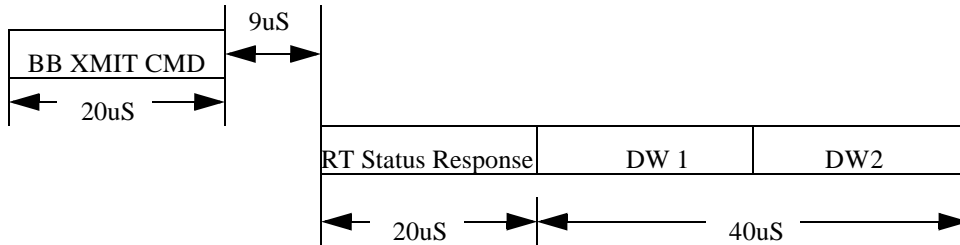
$$\frac{\text{S}\mu\text{MMIT Bus Usage}}{\text{Frame Cycle Time}} = 0.09\% ^*$$

*Note:

To minimize the amount of continuous local bus time the SμMMIT will require, the SμMMIT will be operating in non-buffered mode and have zero wait-states for all memory accesses.

2.2 BB Bus Controller

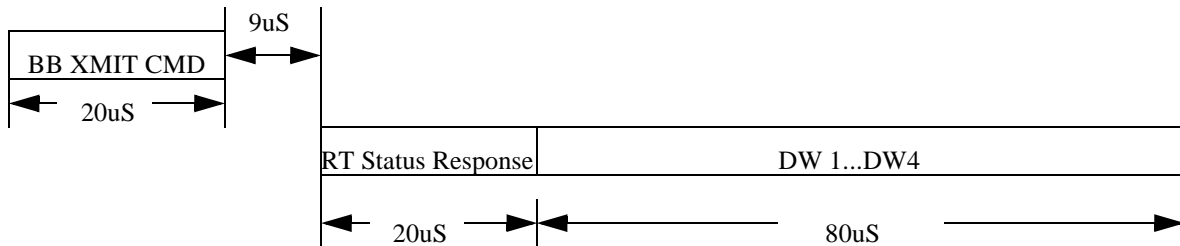
BB sends a Transmit 2 Data Words Command to S/A #3 of RT#1, RT#2 and RT#3 every 200Hz (1/5mS) for Critical Sensor data acquisition.



The duty cycle for the BB 200Hz command is then expressed in terms of bus transmit time over the command repeat duration.

$$\frac{89\mu\text{S}}{5\text{ mS}} = 1.78\% \quad 1.78\% \times 3\text{RT's} = 5.34\%$$

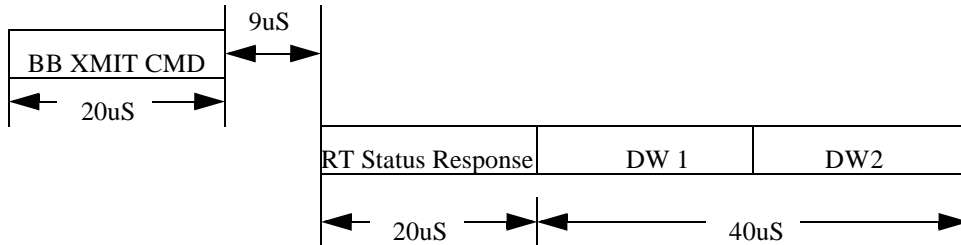
BB sends a Transmit 4 Data Words Command to S/A #2 of RT#1, RT#2 and RT#3 every 100Hz (1/10mS) for House-keeping telemetry items (Battery Voltage, Battery Current, ACS Voltage, Horizon Sensor, Air Pressure and Altimeter).



The duty cycle for the BB 100Hz command is then expressed in terms of bus transmit time over the command repeat duration.

$$\frac{129\mu\text{S}}{10\text{ mS}} = 1.29\% \quad 1.29\% \times 3\text{RT's} = 3.87\%$$

BB sends a Transmit 2 Data Words Command to S/A #1 of RT#2 and RT#3 every 400Hz (1/2.5mS) for actuator position acquisition.

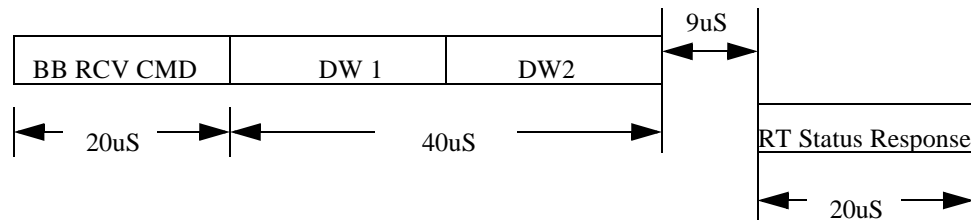


The duty cycle for the BB 400Hz command is then expressed in terms of bus transmit time over the command repeat duration.

$$\frac{89\mu\text{S}}{2.5 \text{ mS}} = 3.56\% \quad 3.56\% \times 2\text{RT}'\text{s} = 7.12\%$$

Finally, consider the BB command for actuator position.

The BB sends a Receive 2 Data Words Command to S/A #1 of RT#2 and RT#3 every 400Hz (1/2.5mS) for actuator position control.



The duty cycle for the BB 400Hz command is then expressed in terms of bus transmit time over the command repeat duration.

$$\frac{89\mu\text{S}}{2.5 \text{ mS}} = 3.56\% \quad 3.56\% \times 2\text{RT}'\text{s} = 7.12\%$$

$$\begin{aligned} \text{Bus Usage} &= 7.12\% + 7.12\% + 3.87\% + 5.34\% \\ &= 23.45\% \end{aligned}$$

The BB BC local bus time required by the SμMMIT versus the 1553 message time is as follows:

$$\frac{[666.72\text{nS (Descriptor Read)} + 166.7\text{nS (Read 2 DW)} + 666.72\text{nS (Descriptor Update)}] \times 3 + 166.7\text{nS (Interrupt log)} \times 3}{5\text{mS (200 Hz cycle time)}}$$

$$\frac{[666.72\text{nS (Descriptor Read)} + 333.36\text{nS (Read 4 DW)} + 666.72\text{nS (Descriptor Update)}] \times 3 + 166.7\text{nS (Interrupt log)} \times 3}{10\text{mS (100 Hz cycle time)}}$$

$$\frac{[666.72 \text{ (Descriptor Read)} + 166.7\text{nS (Read 2 DW)} + 666.72 \text{ (Descriptor Update)}] \times 2 + 166.7\text{nS (Interrupt log)} \times 3}{2.5\text{mS (400 Hz cycle time)}}$$

$$\frac{[666.72 \text{ (Descriptor Read)} + 166.7\text{nS (Read 2 DW)} + 666.72 \text{ (Descriptor Update)}] \times 2 + 166.7\text{nS (Interrupt log)} \times 3}{2.5\text{mS (400 Hz cycle time)}}$$

$$\frac{\text{S}\mu\text{MMIT Bus Usage}}{\text{Frame Cycle Time}} = \frac{17.5\mu\text{S}}{2.5\text{mS}}$$

$$\frac{\text{S}\mu\text{MMIT Bus Usage}}{\text{Frame Cycle Time}} = 0.7\% *$$

*Note:

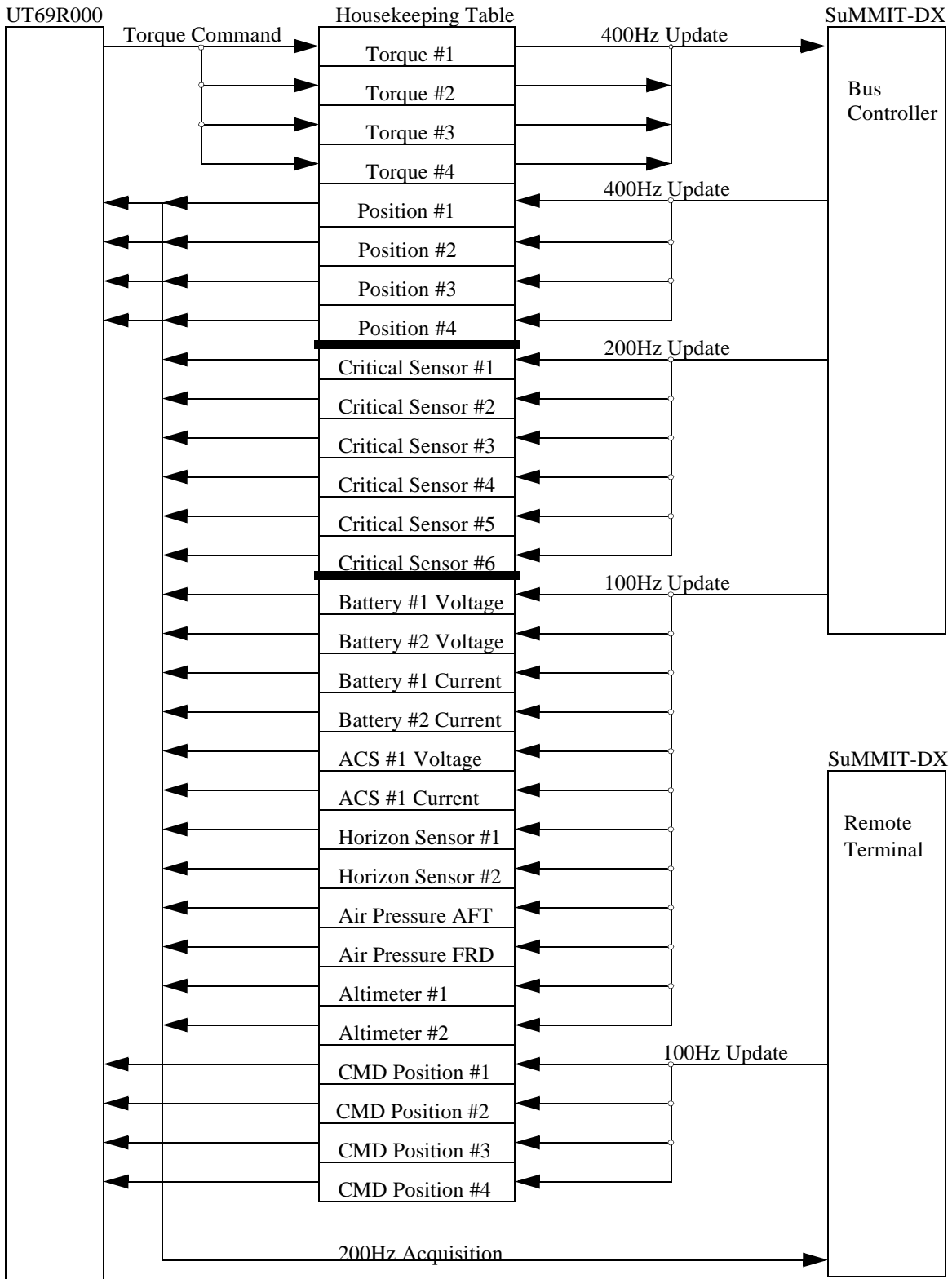
To minimize the amount of continuous local bus time the SμMMIT will require, the SμMMIT will be operating in non-buffered mode and have zero wait-states for all memory accesses.

Bus usage summary:

Accounting for two SμMMIT-DX devices connected to the same local memory bus, (operating in RT and BC mode), with the maximum 1553 Command scenario running simultaneously, the SμMMIT Vs. 1553 Bus time increases to 0.78%. Operating the SμMMIT in the non-buffered mode, distributes more DMA accesses across a broader time range of the overall 1553 message and therefore more local bus accesses. The benefit yielded from this mode of operation is the fact that the Data Word (single word read) DMA access time is greatly reduced. Instead of a (buffered mode) maximum access requirement of 2.167μS (26 Data Words x 41.67nS x2), each SμMMIT demands only 83.33nS for each data word interaction, spaced approximately every 9μS between data word accesses. If both SμMMIT-DX devices align such that each SμMMIT is requesting access at each others respective critical time and the BB processor keeps the bus the maximum* amount of time prior to granting access, the longest bus access time would be as follows: The RT is requesting the longest DMA time of 500.04nS, simultaneously the BC is requesting its maximum DMA time of 666.72nS. Given these conditions, none of the SμMMIT accesses would cause a local bus time-out (7μS RT mode DMA time-out), nor would any processor functions be impeded.

* Note: The R000 processor will grant access to the local memory bus within seven processor clocks (16Mhz x 7 = 438nS).

3.0 Black Box Overview



System Overview

3.2 Data Bus and Control Signals

Now that the basic architecture is established, further definition with respect to the memory mapping of each 1553 protocol device and arbitration logic can be created.

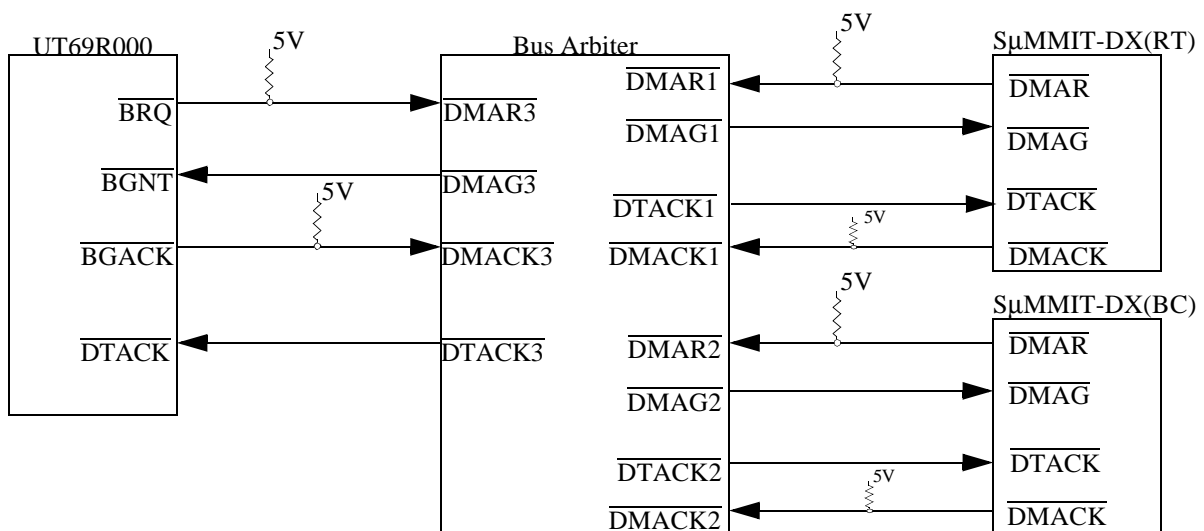
The data bus interface of the R000 is 16 bits wide (D15:D0) and has a (data port) 16 bit address bus (A15:A0). The R000 uses commercially standard types of memory and I/O bus control signals. The control signals are as follows: Memory/Input-Output ($\overline{M/\overline{IO}}$), designates whether the current bus cycle is a Memory (active high), or $\overline{I/O}$ (Active low) operation; $\overline{Read/Write}$ ($\overline{R/\overline{WR}}$), designates whether the current bus cycle is a Read (active high), or \overline{Write} (active low) operation; \overline{DS} , indicates the current bus cycle data is valid (Write), or the addressed (Read) data should be placed on the data bus; \overline{DTACK} indicates the current bus cycle (active low) can be terminated; \overline{BRQ} , Bus Request output pin from the R000 requesting control of the local data bus; \overline{BGNT} , Bus Grant input pin (active low) to the R000, indicates the R000 has been granted control of the local memory bus; \overline{BGACK} , Bus Grant Acknowledge (active low), indicates the R000 has received the Bus Grant signal and is acknowledging local memory bus access. The μ MMIT-DX data bus interface is very similar to the R000's. The μ MMIT data and address busses are 16 bits wide (D15:D0) and (A15:A0) respectively. The μ MMIT control signals are as follows:

Chip Select (\overline{CS}), enables the Host to read or write to the internal μ MMIT registers; $\overline{Read/Write}$ ($\overline{R/\overline{WR}}$), used in conjunction with \overline{CS} to perform a μ MMIT register Read (active high), or \overline{Write} (active low) operation; \overline{RWR} , indicates the current bus cycle data is valid (Write), \overline{RRD} , indicates the current bus cycle data the addressed (Read) data should be placed on the data bus; \overline{RCS} , used in conjunction with \overline{RRD} or \overline{RWR} to perform μ MMIT memory accesses; \overline{DTACK} indicates the current bus cycle (active low) can be terminated; \overline{DMAR} , DMA Request output pin from the μ MMIT requesting control of the local data bus; \overline{DMAG} , DMA Grant input pin (active low) to the μ MMIT, indicates the μ MMIT has been granted control of the local memory bus; \overline{DMACK} , DMA Grant Acknowledge (active low) output pin, indicates the μ MMIT has received and is acknowledging the Bus Grant signal permitting local memory bus access.

3.3 Bus Arbitration

The following describes the arbitration required between both μ MMITs and R000 processor. Since the 1553 is an asynchronous bus and the response is a timed function, the arbiter should provide priority in the following order: 1) 1553 RT, 2) 1553 BC, 3) Local processor.

The arbiter design for this example is contained in Appendix A of this document. The arbitration schematic is provided as a guide and not intended to be used for a final design; issues surrounding timing are application specific and need to be evaluated for each target system. An overview of the arbiter interface is shown below.

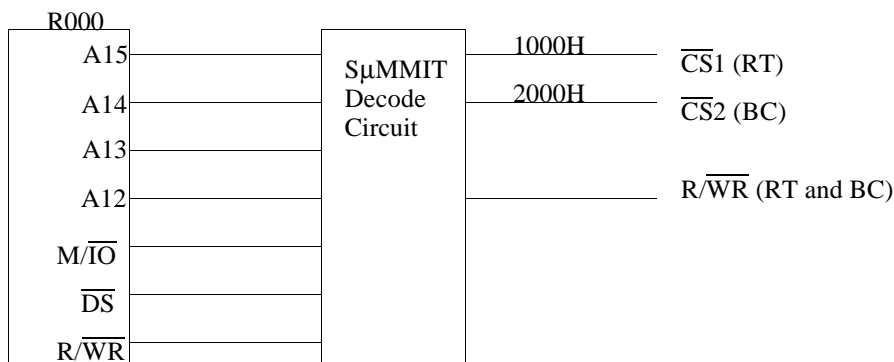


3.4 Memory and I/O Map

The internal registers of the S μ MMIT devices will be selected by an I/O operation from the UT69R000. The S μ MMIT controlling the RT function will have its internal registers mapped starting at location 1000 Hex. The S μ MMIT controlling the BC function will have its internal registers mapped starting at location 2000 Hex.

The I/O address and S μ MMIT registers correlation is as follows:

Register	Physical Address	Function BC Mode	Physical Address	Function RT Mode
0	2000	Control	1000	Control
1	2001	Operational Status	1001	Operational Status
2	2002	Current Command Block	1002	Current Command
3	2003	Interrupt Mask	1003	Interrupt Mask
4	2004	Pending Interrupt	1004	Pending Interrupt
5	2005	Interrupt Log List Pointer	1005	Interrupt Log List Pointer
6	2006	BIT Word	1006	BIT Word
7	2007	Minor Frame Timer	1007	Time Tag
8	2008	Command Block Pointer	1008	SRT Descriptor Pointer
9	2009	Not Used	1009	1553 Status Word Bits
10	200A	Cmd Blk initialization count	100A	Not Used
11	200B	Not Used	100B	Not Used
12	200C	Not Used	100C	Not Used
13	200D	Not Used	100D	Not Used
14	200E	Not Used	100E	Not Used
15	200F	Not Used	100F	Not Used
16	2010	Not Used	1010	Receive
17	2011	Not Used	1011	Receive
18	2012	Not Used	1012	Transmit
19	2013	Not Used	1013	Transmit
20	2014	Not Used	1014	Broadcast Receive
21	2015	Not Used	1015	Broadcast Receive
22	2016	Not Used	1016	Broadcast Transmit
23	2017	Not Used	1017	Broadcast Transmit
24	2018	Not Used	1018	Mode Code Receive
25	2019	Not Used	1019	Mode Code Receive
26	201A	Not Used	101A	Mode Code Transmit
27	201B	Not Used	101B	Mode Code Transmit
28	201C	Not Used	101C	Broadcast Mode Code Receive
29	201D	Not Used	101D	Broadcast Mode Code Receive
30	201E	Not Used	101E	Broadcast Mode Code Transmit
31	201F	Not Used	101F	Broadcast Mode Code Transmit



3.5 Housekeeping Table

Each SμMMIT will have a region of local memory dedicated for descriptor space. To maximize performance and minimize data manipulation, the Housekeeping Table will be located within a common address range (8000-801D).

Address (Hex)	Housekeeping Table Function
8000	Torque #1
8001	Torque #2
8002	Torque #3
8003	Torque #4
8004	Position #1
8005	Position #2
8006	Position #3
8007	Position #4
8008	Critical Sensor #1
8009	Critical Sensor #2
800A	Critical Sensor #3
800B	Critical Sensor #4
800C	Critical Sensor #5
800D	Critical Sensor #6
800E	Battery #1 Voltage
800F	Battery #2 Voltage
8010	Battery #1 Current
8011	Battery #2 Current
8012	ACS #1 Voltage
8013	ACS #1 Current
8014	Horizon Sensor #1
8015	Horizon Sensor #2
8016	Air Pressure AFT
8017	Air Pressure FRD
8018	Altimeter #1
8019	Altimeter #2
801A	CMD Position #1
801B	CMD Position #2
801C	CMD Position #3
801D	CMD Position #4

4.0 Black Box 1553 Software Initialization

4.1 Black Box configuration setup for the Bus Controller initialization.

Black Box Bus Controller Command Block listing for Minor and Major Frames.

Below is an overview of the BC mode command block structure. Each command block requires an allocation of 8 memory locations.

Bus Controller Command Block Format

Address Function

0000	Control Word
0001	Command Word 1
0002	Command Word 2
0003	Data Pointer
0004	Status Word 1
0005	Status Word 2
0006	Branch Address
0007	Timer Value

Command Block Execution:

Once it has been granted access ($\overline{DMAG}=0$) to the local memory bus, the μ MMIT will read all eight words of the command block from memory in a single burst. The μ MMIT decodes the Command Block control word and performs the instructed operations. Once the appropriate action has been taken, the μ MMIT performs an update of the command block through another DMA burst into memory. If interrupts were enabled and an interrupt condition occurred, there would be a total of eight words (Control Word, Command Word 1, Command Word 2, Data Pointer, Status Word 1, Status Word 2, Interrupt Status Word and Interrupt Address Word) written into memory during the Command Block update. If interrupts were enabled but no interrupt condition occurred, there would be a total of six words (Control Word, Command Word 1, Command Word 2, Data Pointer, Status Word 1 and Status Word 2) written into memory during the Command Block update. In certain cases, the μ MMIT will not perform a command block update prior to continuing to the next command block; these opcodes (that don't require the command block update) are listed below.

EOL (end of List), Skip, Go To, Built-in Test, Interrupt and Continue, Call, Return to Call, LMFT (Load Minor Frame Timer) and Return to Branch.

If interrupts are enabled, the op-codes that generate interrupts will cause a two word (Interrupt Status Word and Interrupt Address Word) burst update at the end of message processing.

For further information regarding the μ MMIT Command Block execution refer to the latest Enhanced μ MMIT Family Product Handbook.

4.2 Bus Controller Command Block Listing

For this application, the BC Command blocks will be located at address 2100 Hex (Top of Command Block) and will be initialized by the R000 processor after a system reset. The following list of Command Blocks are the minimum required to perform the required BB Bus Controller function. The Command Block listing could easily be used as a skeleton for a more elaborate Bus Controller command structure, utilizing more of the autonomous μ MMIT features.

After Reset, the R000 writes the following values to the local memory to initialize the BC Command blocks.

BB Major Frame

Executes 3 minor Frames of 100Hz, 200Hz and 400Hz

[Command Block 1] 400Hz Minor Frame Start

Address	Data	Function
2100	E000	Load Minor Frame Timer
2101	0000	1553 Command 1 (not applicable)
2102	0000	1553 Command 2 (not applicable)
2103	0000	Data address pointer (not applicable)

2104	0000	Status Word 1
2105	0000	Status Word 2
2106	0000	Branch address
2107	0027	Minor Frame Timer value = 2.5mS (64uS/bit) for 400Hz. Note: 62.5nS under 2.5mS.

[Command Block 2] Sample Actuator positions 1 and 2

Address	Data	Function
2108	4200	Execute and continue
2109	1422	1553 Command: RT#2, Transmit, SA#1, Data words = 2, Bus=A
210A	0000	1553 Command 2 (not applicable)
210B	8004	Data address pointer (Housekeeping Table)
210C	0000	Status Word 1
210D	0000	Status Word 2
210E	0000	Branch address
210F	0000	Timer value

[Command Block 3] Sample Actuator positions 3 and 4

Address	Data	Function
2110	4200	Execute and continue
2111	1C22	1553 Command: RT#3, Transmit, SA#1, Data words = 2, Bus=A
2112	0000	1553 Command 2 (not applicable)
2113	8006	Data address pointer (Housekeeping Table)
2114	0000	Status Word 1
2115	0000	Status Word 2
2116	0000	Branch address
2117	0000	Timer value

[Command Block 4] Send Torque Commands 1 and 2

Address	Data	Function
2118	4200	Execute and continue
2119	1022	1553 Command: RT#2, Receive, SA#1, Data words = 2, Bus=A
211A	0000	1553 Command 2 (not applicable)
211B	8000	Data address pointer (Housekeeping Table)
211C	0000	Status Word 1
211D	0000	Status Word 2
211E	0000	Branch address
211F	0000	Timer value

[Command Block 5] Send Torque Commands 3 and 4

Address	Data	Function
2120	4200	Execute and continue
2121	1822	1553 Command: RT#3, Receive, SA#1, Data words = 2, Bus=A
2122	0000	1553 Command 2 (not applicable)
2123	8002	Data address pointer (Housekeeping Table)
2124	0000	Status Word 1
2125	0000	Status Word 2
2126	0000	Branch address
2127	0000	Timer value

[Command Block 6] Send Interrupt to the R000 to alert the completion of the 400Hz Minor Frame

Address	Data	Function
2128	A000	Interrupt and continue
2129	0000	1553 Command 1 (not applicable)
212A	0000	1553 Command 2 (not applicable)
212B	0000	Data address pointer (not applicable)
212C	0000	Status Word 1
212D	0000	Status Word 2
212E	0000	Branch address
212F	0000	Timer value

[Command Block 7] Frame selection occurs here (Back to top of 400Hz MF, or continue to 200Hz MF)

Address	Data	Function
2130	2000	GOTO
2131	0000	1553 Command 1 (not applicable)
2132	0000	1553 Command 2 (not applicable)
2133	0000	Data address pointer (not applicable)
2134	0000	Status Word 1
2135	0000	Status Word 2
2136	2100	Branch address - The first time through, send the S μ MMIT back to the beginning of the 400Hz MF
2137	0000	Timer value

200Hz Minor Frame Start

[Command Block 1] Sample Critical Sensors 1 and 2

Address	Data	Function
2138	4200	Execute and continue
2139	0C62	1553 Command: RT#1, Transmit, SA#3, Data words = 2, Bus=A
213A	0000	1553 Command 2 (not applicable)
213B	8008	Data address pointer (Housekeeping Table)
213C	0000	Status Word 1
213D	0000	Status Word 2
213E	0000	Branch address
213F	0000	Timer value

[Command Block 2] Sample Critical Sensors 3 and 4

Address	Data	Function
2140	4200	Execute and continue
2141	1462	1553 Command: RT#2, Transmit, SA#3, Data words = 2, Bus=A
2142	0000	1553 Command 2 (not applicable)
2143	800A	Data address pointer (Housekeeping Table)
2144	0000	Status Word 1
2145	0000	Status Word 2
2146	0000	Branch address
2147	0000	Timer value

[Command Block 3] Sample Critical Sensors 5 and 6

Address	Data	Function
2148	4200	Execute and continue
2149	1C62	1553 Command: RT#3, Transmit, SA#3, Data words = 2, Bus=A
214A	0000	1553 Command 2 (not applicable)
214B	800C	Data address pointer (Housekeeping Table)
214C	0000	Status Word 1
214D	0000	Status Word 2
214E	0000	Branch address
214F	0000	Timer value

[Command Block 4] Send Interrupt to the R000 to alert the completion of the 200Hz Minor Frame

Address	Data	Function
2150	A000	Interrupt and continue
2151	0000	1553 Command 1 (not applicable)
2152	0000	1553 Command 2 (not applicable)
2153	0000	Data address pointer (not applicable)
2154	0000	Status Word 1
2155	0000	Status Word 2
2156	0000	Branch address
2157	0000	Timer value

[Command Block 5] Frame selection occurs here (Back to top of 400Hz MF, or continue to 100Hz MF).

Address	Data	Function
2158	2000	GOTO
2159	0000	1553 Command 1 (not applicable)
215A	0000	1553 Command 2 (not applicable)
215B	0000	Data address pointer (not applicable)
215C	0000	Status Word 1
215D	0000	Status Word 2
215E	2100	Branch address - The first time through, send the S μ MMIT back to the beginning of the 400Hz MF
215F	0000	Timer value

100Hz Minor Frame Start

[Command Block 1] Sample Battery 1-2 Voltage and Current

Address	Data	Function
2160	4200	Execute and continue
2161	0C44	1553 Command: RT#1, Transmit, SA#2, Data words = 4, Bus=A
2162	0000	1553 Command 2 (not applicable)
2163	800E	Data address pointer (Housekeeping Table)
2164	0000	Status Word 1
2165	0000	Status Word 2
2166	0000	Branch address
2167	0000	Timer value

[Command Block 2] Sample ACS and Horizon sensors

Address	Data	Function
2168	4200	Execute and continue
2169	1444	1553 Command: RT#2, Transmit, SA#2, Data words = 4, Bus=A
216A	0000	1553 Command 2 (not applicable)
216B	8012	Data address pointer (Housekeeping Table)
216C	0000	Status Word 1
216D	0000	Status Word 2
216E	0000	Branch address
216F	0000	Timer value

[Command Block 3] Sample Air Pressure and Altimeter sensors

Address	Data	Function
2170	4200	Execute and continue
2171	1C44	1553 Command: RT#3, Transmit, SA#2, Data words = 4, Bus=A
2172	0000	1553 Command 2 (not applicable)
2173	8016	Data address pointer (Housekeeping Table)
2174	0000	Status Word 1
2175	0000	Status Word 2
2176	0000	Branch address
2177	0000	Timer value

[Command Block 4] Send Interrupt to the R000 to alert the completion of the 100Hz Minor Frame

Address	Data	Function
2178	A000	Interrupt and continue
2179	0000	1553 Command 1 (not applicable)
217A	0000	1553 Command 2 (not applicable)
217B	0000	Data address pointer (not applicable)
217C	0000	Status Word 1
217D	0000	Status Word 2
217E	0000	Branch address
217F	0000	Timer value

[Command Block 5] Always return to top of 400Hz MF.

Address	Data	Function
2180	2000	GOTO
2181	0000	1553 Command 1 (not applicable)
2182	0000	1553 Command 2 (not applicable)
2183	0000	Data address pointer (not applicable)
2184	0000	Status Word 1
2185	0000	Status Word 2
2186	2100	Branch address - Send the SμMMIT back to the beginning of the 400Hz MF
2187	0000	Timer value

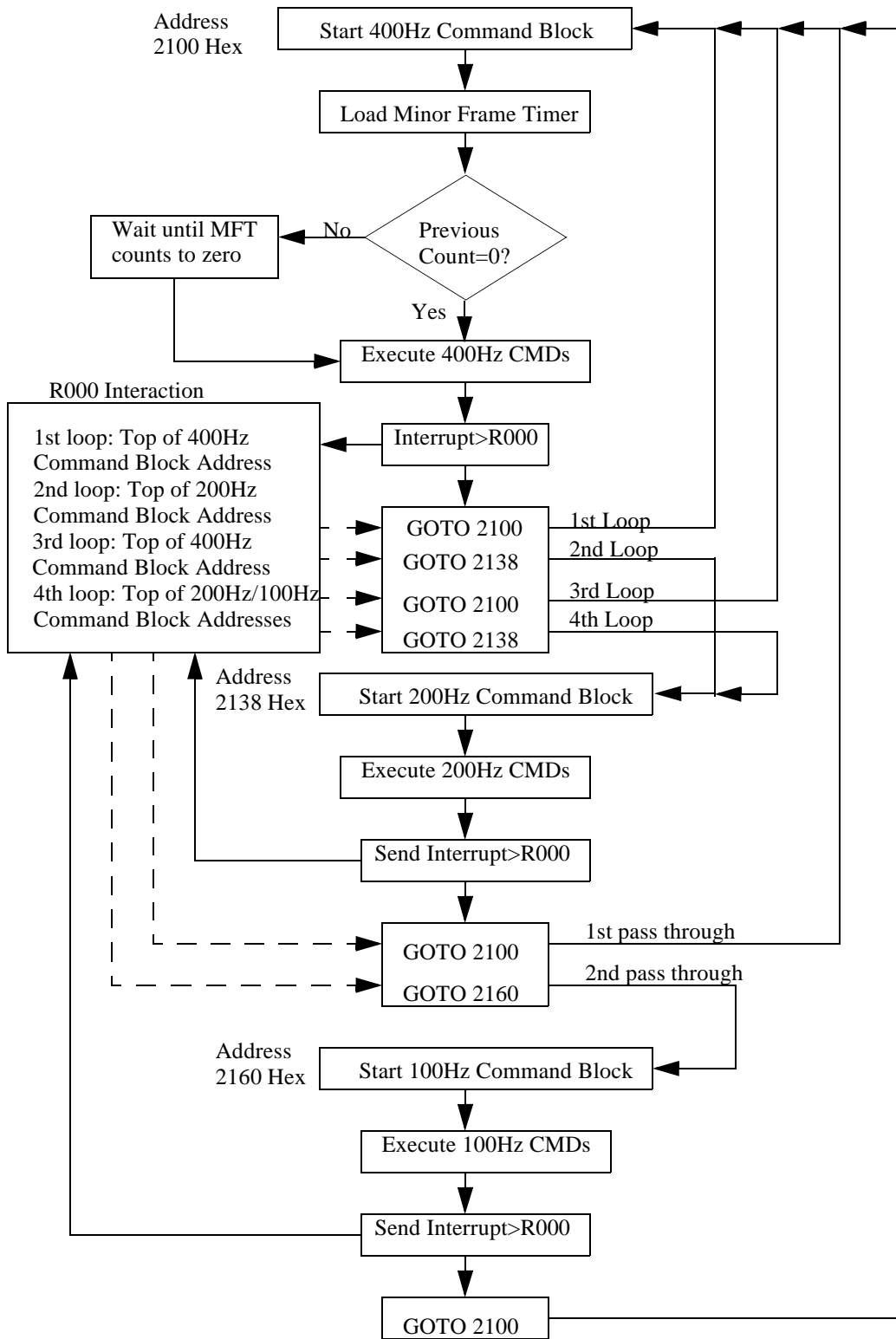
4.3 Bus Controller Register Setup.

After Reset, the R000 writes the following values to the internal registers of the SμMMIT to initialize and begin the BC mode of operation.

	Address	Data	
R000 write >	2003	0002	Interrupt Mask = [Enable CBA Interrupt]
R000 write >	2005	2200	Interrupt Log List Pointer= Address 2200 Hex
R000 write >	2008	2100	Command Block Pointer = [400Hz Command Block 1]
R000 write >	2000	8002	Control Register = [Start Execution, Enable Interrupt Logging]

As the SμMMIT executes the Command Blocks, the R000 waits for the MSG_INT to occur. The interrupt serves two purposes; to synchronize the R000 with the 1553 command blocks and to alert the R000 as to where within the Major Frame the Bus Controller is currently executing. The R000 modifies the jump location to select the appropriate Minor Frame execution path. The following diagram illustrates the Minor Frame execution path and the R000 interaction based upon the interrupts.

4.4 Bus Controller Command Execution Flow Chart.



4.5 Remote Terminal Descriptor Format.

Below is an overview of the RT mode Descriptor block structure. Each S/A requires an allocation of 4 memory locations for the associated RT descriptor. The RT descriptor space will be located in local memory starting at address 1100 Hex.

Remote Terminal and Mode Code Descriptor Format (Using Mode 2)

Address Function

0000	Control Word
0001	Top Address
0002	Current Address
0003	Message Information Buffer Address

The Remote Terminal Descriptor execution is as follows:

Once it has been granted access ($\overline{\text{DMAG}}='0'$) to the local memory bus, the μMMIT will read all four words of the descriptor block from memory in a single burst. The μMMIT decodes the Control word and reacts to the received 1553 message based on the Descriptor information. Once the 1553 message is complete, the μMMIT performs an update of the Descriptor block and Message Information Buffer through another DMA burst into memory. If interrupts were enabled and an interrupt condition occurred, there would be a total of six words (Message Information Word, Time Tag, Current Address, Control Word, Interrupt Information Word and Interrupt Address Word) written into memory during the Descriptor Block and MIB update. If interrupts were enabled but no interrupt condition occurred, there would be a total of four words (Message Information Word, Time Tag, Current Address, Control Word) written into memory during the Descriptor Block and MIB update. For further information regarding the μMMIT Descriptor Block and Message Information Buffer, refer to the latest Enhanced μMMIT Family Product Handbook.

4.6 Remote Terminal Descriptor Listing

For this application, the RT Descriptor blocks will be located at address 1100 Hex (Top of Descriptor Space) and will be initialized by the R000 processor after a system reset.

After Reset, the R000 writes the following values to the local memory to initialize the RT Descriptor space. The only S/A's and Mode Codes that are initialized are the ones used; all others (not used) are illegalized and therefore will be initialized to all zeros.

Descriptor Block Initialization

[S/A1 1553 Receive Command]

Address	Data	Function
1104	0140	Control Word Set buffer to wrap after one message, set IWA bit to true.
1105	801A	Top Address Point to the 1st (top) Torque Command
1106	801A	Current Address
1107	0000	Message Information Buffer Address

[S/A1 1553 Transmit Command]

Address	Data	Function
1184	0140	Control Word Set buffer to wrap after one message, set IWA bit to true.
1185	8000	Top Address Point to the Top of the Housekeeping Table
1186	8000	Current Address
1187	0004	Message Information Buffer Address

[S/A2 1553 Transmit Command]

Address	Data	Function
1188	0140	Control Word Set buffer to wrap after one message, set IWA bit to true.
1189	F777	Top Address Point to the system status word
118A	F777	Current Address
118B	0008	Message Information Buffer Address

[1553 Receive Mode Code Command with Data]

Address	Data	Function
1204	0140	Control Word Set buffer to wrap after one message, set IWA bit to true.
1205	001A	Top Address Storage buffer for the received time tag word (Synchronize MC with Data)
1206	001A	Current Address
1207	000C	Message Information Buffer Address

4.7 Remote Terminal Register Setup

After Reset, the R000 writes the following values to the internal registers of the SμMMIT to initialize and begin the RT mode of operation.

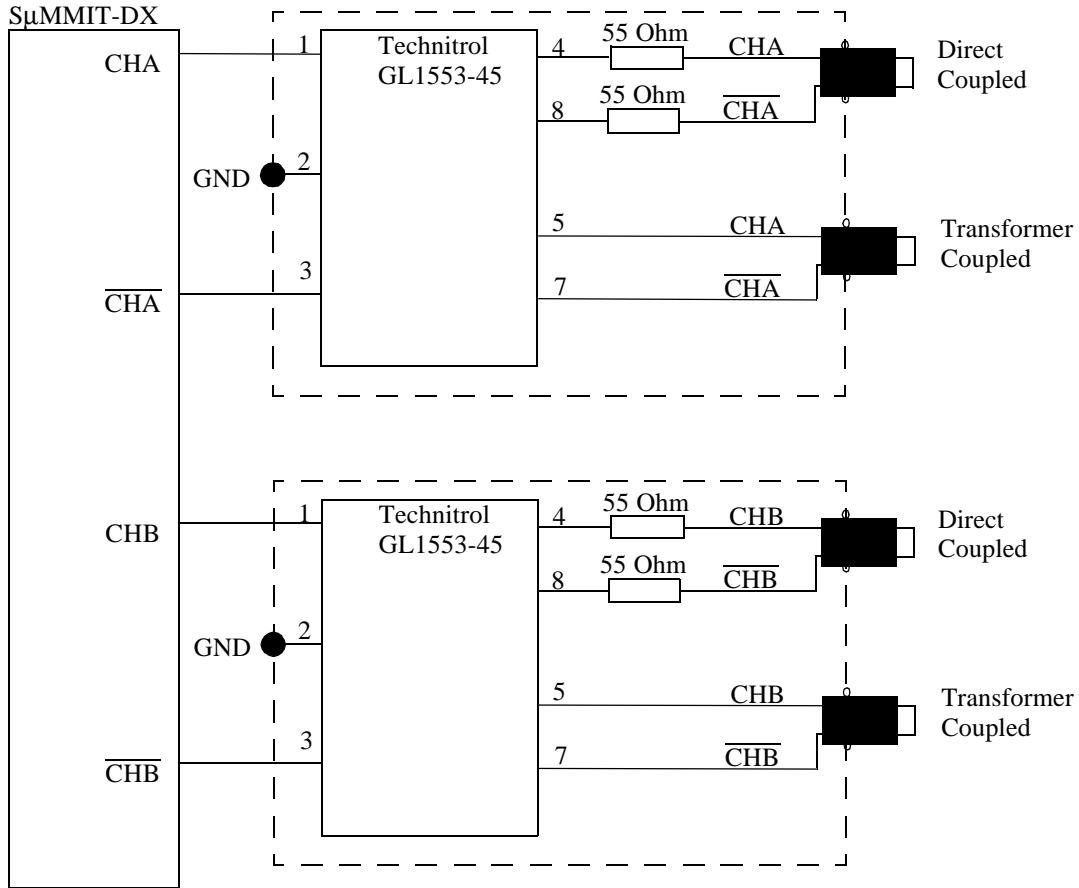
	Address	Data	
R000 write >	1003	0400	Interrupt Mask = [Enable S/A accessed Interrupt]
R000 write >	1005	1400	Interrupt Log List Pointer= Address 1400 Hex
R000 write >	1008	1100	Remote Terminal Descriptor Block Pointer = [S/A0 1553 Receive Command]
R000 write >	1010	FF7D	Illegalization Register = [Receive S/A 1 Legal, 0, 2-15 Illegal]
R000 write >	1011	FFFF	Illegalization Register = [Receive S/A 16-31 Illegal]
R000 write >	1012	FFF9	Illegalization Register = [Transmit S/A 1 and 2 Legal, 0, 3-15 Illegal]
R000 write >	1013	FFFF	Illegalization Register = [Transmit S/A 16-31 Illegal]
R000 write >	1014	FFFF	Illegalization Register = [Receive Broadcast S/A 0-15 Illegal]
R000 write >	1015	FFFF	Illegalization Register = [Receive Broadcast S/A 16-31 Illegal]
R000 write >	1018	FFFF	Illegalization Register = [Receive Mode Code S/A 1 Legal, 0 and 2-15 Illegal]
R000 write >	1019	FFFF	Illegalization Register = [Receive Mode Code S/A 16-31 Illegal]
R000 write >	101A	FFFF	Illegalization Register = [Transmit Mode Code S/A 0-15 Illegal]
R000 write >	101B	FFFF	Illegalization Register = [Transmit Mode Code S/A 16-31 Illegal]
R000 write >	101C	FFFF	Illegalization Register = [Broadcast Receive Mode Code S/A 0-15 Illegal]
R000 write >	101D	FFFF	Illegalization Register = [Broadcast Receive Mode Code S/A 16-31 Illegal]
R000 write >	101E	FFFF	Illegalization Register = [Broadcast Transmit Mode Code S/A 0-15* Illegal]
R000 write >	1000	9982	Control Register = [Start Execution, Enable Interrupt Logging, CH A&B enabled] [MODE 2 selected]

* Note: SμMMIT will be operating in 1553B mode only, therefore the Broadcast Transmit Mode Code S/A 16-31 are internally illegalized by the SμMMIT.

The SμMMIT responds to the incoming 1553 commands and since the interrupt when accessed bit is set for legal S/A and Mode Codes, alerting the R000 to each message transfer.

5.0 1553 Bus Interface

The board layout should place the SuMMIT-DX close to the 1553 transformer, locate the transformer close to the 1553 bus connector and eliminate ground and power planes from beneath the transformer. An example layout is illustrated below.



Appendix A

VHDL description for priority encoder

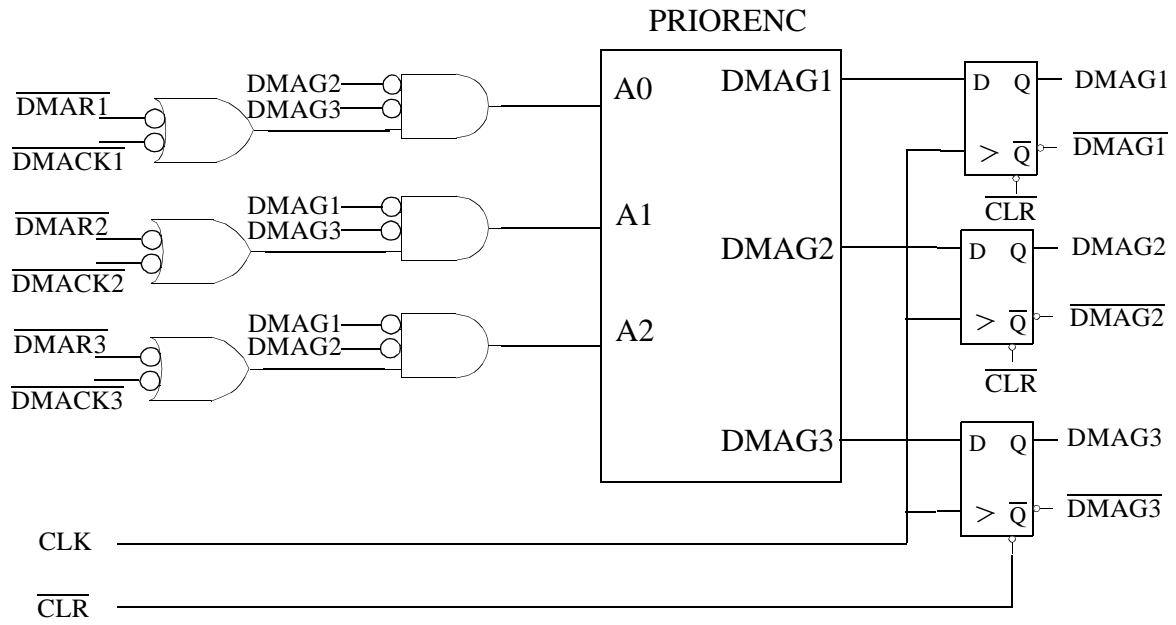
```
package PRIORITY is
-- declare a 3 x 8 Array called ORDER
constant ORDER_WIDTH: INTEGER:= 3;
subtype ORDER_WORD is BIT_VECTOR (1 to ORDER_WIDTH);
subtype ORDER_RANGE is INTEGER range 0 to 7;
type ORDER_TABLE is array (0 to 7) of ORDER_WORD;
constant ORDER: ORDER_TABLE:= ORDER_TABLE'(
"000", -- 000
"001", -- 001
"010", -- 010
"001", -- 011
"100", -- 100
"001", -- 101
"010", -- 110
"001"); -- 111
end PRIORITY;

use PRIORITY.all;

entity priorenc is
port(addr: in ORDER_RANGE;
      data: out ORDER_WORD);
end;

architecture behavior of priorenc is
begin
  data <= ORDER(addr);
end behavior;
```

Bus Arbitration Logic Schematic



Appendix B

BB Remote Terminal S/A 2 data word format

Bit 0: RT#1 SSF (Sub-System Fail)

Bit 1: RT#1 SRQ (Service Request)

Bit 2: RT#1 INS (Instrumentation)

Bit 3: RT#1 TF (Terminal Flag)

Bit 4: RT#2 SSF (Sub-System Fail)

Bit 5: RT#2 SRQ (Service Request)

Bit 6: RT#2 INS (Instrumentation)

Bit 7: RT#2 TF (Terminal Flag)

Bit 8: RT#3 SSF (Sub-System Fail)

Bit 9: RT#3 SRQ (Service Request)

Bit A: RT#3 INS (Instrumentation)

Bit B: RT#3 TF (Terminal Flag)

