

DC Testing Guidelines for NON-JTAG Arrays



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INTRODUCTION

As designs become more complex, testing DC threshold voltage levels for input buffers becomes more difficult. To ensure a complete and correct test is implemented, UTM C has specific requirements for all gate array designs.

UTM C requires all non-JTAG¹ designs to contain a tree (e.g., NAND, XNOR, XOR, etc.) for DC V_{IL} and V_{IH} testing and include a separate set of test patterns to drive the tree. The patterns allow input DC levels to be tested quickly and accurately while minimizing the impact of test noise.

This document describes the NAND tree implementation. You are free to make any necessary changes or use any tree which allow input DC levels to be tested separately.

DC TREE CONSTRUCTION

You can build a NAND tree using NAND2s daisy-chained together similar to that of figure 1. Gates with three or more inputs (NAND3s through NAND8s) may also be used. Connect all input buffers to the NAND tree structure by using output signals of the input buffers. To maintain completeness, bidirectional I/O buffers must also be included in the tree designs (the bidirectional I/O must be set to the input mode during testing).

For transparency in the normal operating mode, you can use one of three simple techniques to integrate a tree circuit into your chip design:

- Add one pin for DC test output and one pin for DC test control.
- Apply an unused opcode or mode for DC test configuration.
- Use a master reset signal to initiate the DC test mode.

Two-Pin Technique

Use one input pin to drive all bidirectional buffers into a high-impedance/input mode. Use a second pin as a NAND tree output for test result verification. Use this implementation when extra pins are available on the selected package.

Unused Opcode Technique

This technique eliminates extra pin requirements. By applying an unused opcode, all bidirectional pins are forced into a high-impedance state, exercising the bidirectional input path. In addition, the opcode selects a MUX path connecting the NAND tree to the appropriate output pin.

Master Reset Technique

Using the master reset is an easy method for initiating the tree circuit without changing design functionality. When the reset line is held active, all bidirectional buffers are forced into a high-impedance state. The reset signal also selects the proper MUX path to the output pin. When the reset signal becomes low, the chip is not only completely reset, but is out of the DC test mode.

WRITING TEST PATTERNS

The actual patterns for DC tests are relatively simple to write. Regardless of your choice of technique, you should enable the DC test mode after initialization. Once in the DC test mode, apply input signals so that all non-chained inputs are logical zeros (logical 1 on the associated pad in figure 1). Starting with the NAND gate closest to the test output, set the non-chained input(s) on this gate to 1. Toggle each individual input to 0, then back to 1, remaining at 1 for duration of the test. Repeat this procedure for the next closest gate to the output, and so on, until all the buffers have been tested.

These test patterns must be a separate test on your workstation. Run TRC analysis in LH mode to verify that these patterns work correctly under best-, and worst-case conditions.

For easier routing during layout, UTM C recommends that the connection of NAND gates follow, as closely as possible, the order of pads on the die (see figure 1).

Note:

1. JTAG is the testability practice extracted from IEEE Standard 1149.1, which uses boundary-scan techniques for data manipulation. A chip implementing JTAG standards is not required to use a tree circuit because of the boundary-scan properties employed.

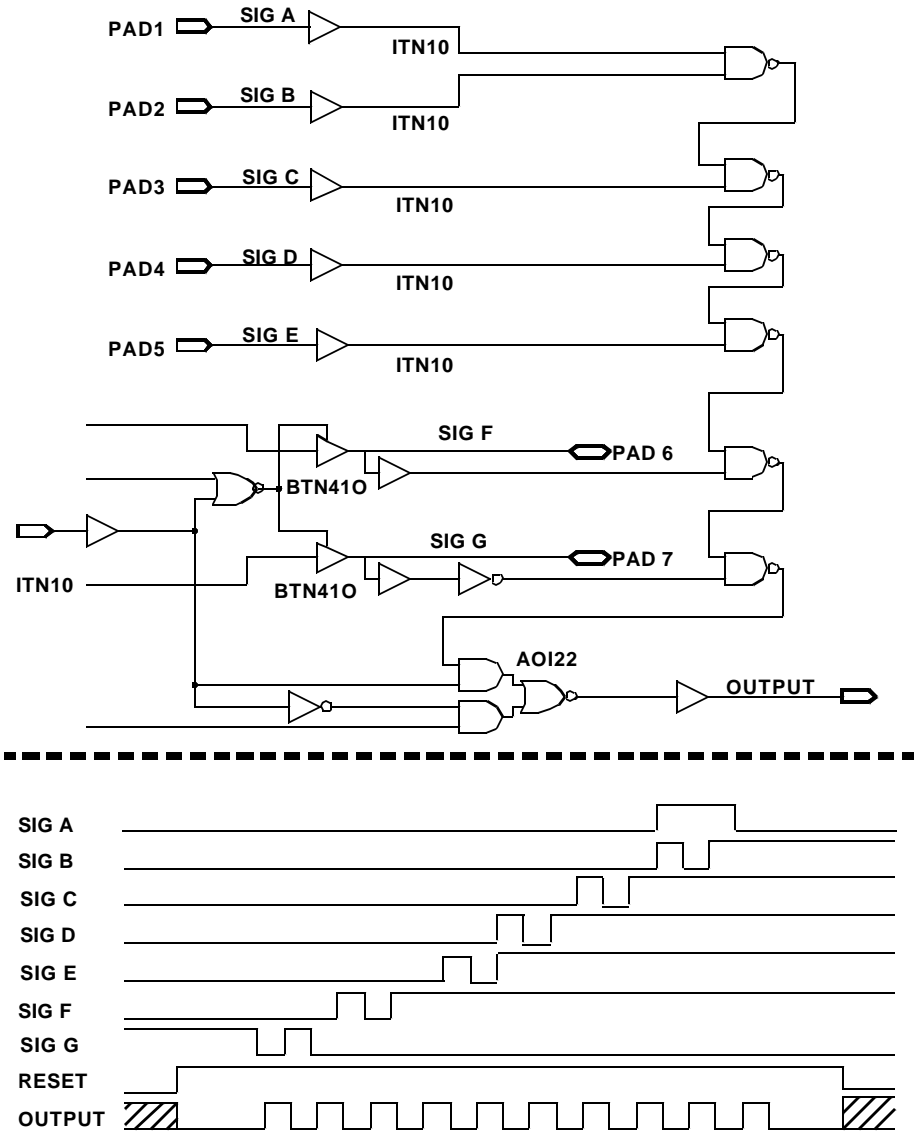


Figure 1. Tree Circuit and Waveforms for DC Testing

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