

UTMC APPLICATION NOTE

Enhanced S μ MMIT Ping-Pong Feature

When enabling and disabling ping-ponging, the act of enabling or disabling must be observed via the acknowledge bit. If no acknowledge is seen, the user MUST make another attempt at enabling or disabling.

Example of ping-pong usage:

Step	Control Register Bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	Start execution	1	x	x	x	x	x	0	x	x	x	x	x	x	1	x	x
2	Read result of Start w/PP	1	x	x	x	x	x	1	x	x	x	x	x	x	1	x	x
3	Disable of PP	1	x	x	x	x	x	1	x	x	x	x	x	x	0	x	x
4	Read result of disable	1	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x
5	Enable of PP	1	x	x	x	x	x	0	x	x	x	x	x	x	1	x	x
6	Read result of enable	1	x	x	x	x	x	1	x	x	x	x	x	x	1	x	x

Step	Control Register Bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	Disable of PP (just after internal μ C has copied control register)	1	x	x	x	x	x	1	x	x	x	x	x	x	0	x	x
2	Read result of disable (no acknowledge, must retry)	1	x	x	x	x	x	1	x	x	x	x	x	x	1	x	x

Step	Control Register Bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	Enable of PP (just after internal μ C has copied control register)	1	x	x	x	x	x	0	x	x	x	x	x	x	1	x	x
2	Read result of enable (no enable, must retry)	1	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x

The maximum time between enable/disable attempt and observed result is about 32μ S. When writing to enable/disable, the user reads the acknowledge bit reflecting the last machine state, e.g., if enabled, bit 9 = 1, if disabled, 9 = 0.

Example: Bit 9 of the control register is meant to be read only, but can be written to. Do not write to Bit 9.

Step	Control Register Bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	Start execution	1	x	x	x	x	x	0	x	x	x	x	x	x	1	x	x
2	Read result of Start w/PP	1	x	x	x	x	x	1	x	x	x	x	x	x	1	x	x
3	Disable of PP (Writing Bit 9)	1	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x
4	Read back	1	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x
5	Read back 32μ S later	1	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x
6	When did the SuMMIT acknowledge? Can't tell																

Do you have to wait 32μS? No, not always. The user should poll for acknowledge.

Step	Control Register Bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	Disable PP	1	x	x	x	x	x	1	x	x	x	x	x	x	0	x	x
2	Read back (enabled)	1	x	x	x	x	x	1	x	x	x	x	x	x	0	x	x
3	Read back 32μS later (worst case)	1	x	x	x	x	x	0	x	x	x	x	x	x	0	x	x

What if we don't see acknowledge? You'll be able to tell right away if an acknowledge is coming or not.

Step	Control Register Bits	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	Disable PP	1	x	x	x	x	x	1	x	x	x	x	x	x	0	x	x
2	Read back	1	x	x	x	x	x	1	x	x	x	x	x	x	1	x	x
3	In this case, the users write was overwritten; the user must re-write and look for acknowledge.																