

# Application Note



## **Detecting 0° / 180° anomaly on ACT5028 RDC chip using an FPGA**

This application note describes how an FPGA/PLD State Machine design can be implemented to detect an error condition that may occur on the ACT5028 Revision A & B Resolver to Digital Converter. The potential for this problem only occurs when the RDC chip is used in the 16 Bit mode.

There are two modes of failure that can occur when in the 16 bit mode, the details are available in the data sheet and brief description is presented below.

- 1) The RDC counter can lock up 180° out of phase with the input angle presented to the RDC. This condition can only be cleared when the input to the RDC is changed such that the RDC counter is incremented or decremented by one count.
- 2) The RDC counter can jump 180° out of phase (with out locking up) when crossing 0° or 180° and the RDC chip corrects itself at its maximum angular velocity that is set by an external resistor.

## Theory

The method that will be used to determine if one of the two failure modes mentioned above exist would require the reading of the RDC counter at a specific rate and measuring the count difference (LRDC new count - RA last good stored count) to determine if the maximum angular velocity has been exceeded. Figure 1 shows the basic flow of the required states to perform this function.

For example if the maximum angular velocity is 1 revolution per second ( $2^{16}$  counts/S) and the sample rate is a maximum of 3.90625ms, the count difference can not be greater than 256 ( $2^{16} \times 3.9025\text{ms}$ ) between samples. If the count is above 256 the resolver must have an error because the resolver has a maximum angular velocity that was exceeded. If one of the error conditions described above occurs the actual count difference would be 32,768 which is much larger than the 256 count window.

When the error condition is present an Error Flag will be true and stay true until the State Machine reads a value that is within 256 counts of the last good count that is stored in register RA.

If the error was caused by failure mode 2 the Error Flag duration would be  $= \frac{1}{2} \times 1/\text{rps}$  (500ms). If the error was caused by failure mode 1 the Error Flag duration would last as long as failure mode 2 + the time it takes the input to the RDC chip to change.

## State Machine Requirements:

- a) Three bit State Counter (8 States)  
It is assumed that the clocking rate is 1Mhz or higher so that the sequencing of the State machine is insignificant as compared to the delay that is developed by the internal counter.
- b) Power On Rest Circuit (POR)  
This circuit is required to insure that the State Machine begins operation with stable power applied.
- c) One Output  
The Error Flag is to identify when an Error condition exists.
- d) Nine Inputs;  
To simplify the logic only the 9 most significant bits from the RDC chip are required in the calculation to determine if one of the errors occurred. The inputs must be latched to insure stable data and should be synchronous to the State Machine.
- e) Register RA  
RA is 9 bit register that gets loaded from the LRDC register and stores the 9 most significant bits of the last good count read from RDC Counter.
- f) Circuit to Compare new inputs (LRDC) and last good input (RA)  
The Boolean equation to determine the maximum angle difference is;

$$\overline{\text{LRDC}(\text{B16}:\text{B8}) \text{ Xored } \text{RA}(\text{B16}:\text{B8})} \text{ or } \overline{\text{LRDC}(\text{B16}:\text{B7}) \text{ Xored } \text{RA}(\text{B16}:\text{B7})}$$

The left part of the equation is for all angles and the right side of the equation is to account for successive readings that may traverses around zero degrees.

This equation is based on the example above that dictates that the count difference will be no more than 256 counts ( $2^8$ ) within 3.90625ms.

g) Delay Circuit

A counter will be used to produce a delay between reads from the RDC Counter. In the example above a maximum delay of 3.90625ms is required. The delay is not critical and the equation above will still be valid even if the delay was 0.39ms. Keep in mind that the actual error condition that exists is when the count error jumps 32,768 counts ( $\frac{1}{2} \times 2^{16}$ ). When the delay is decreased the Error Flag will trip at a higher angular velocity. This counter should be reset to all zeros when not in State 5 and allowed to run when State 5 is entered.

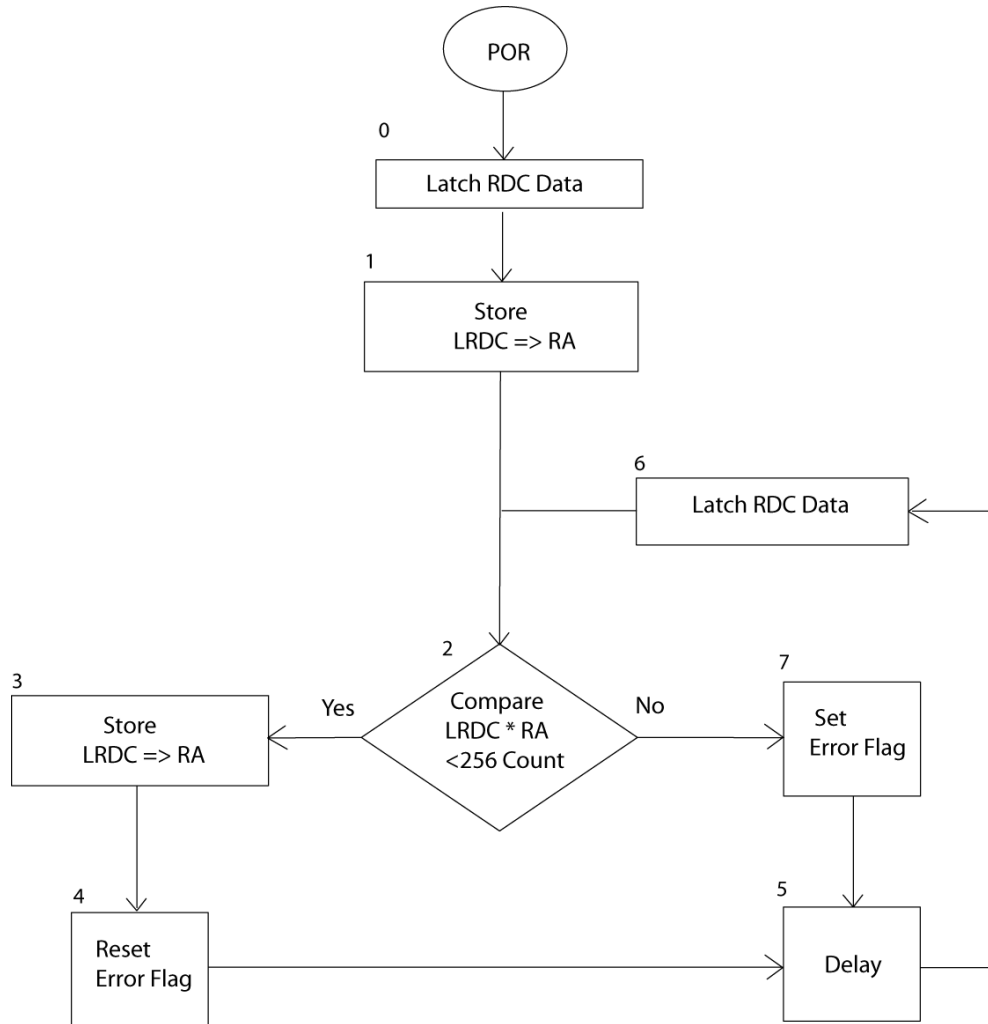


Figure 1

**PLAINVIEW, NEW YORK**  
 Toll Free: 800-THE-1553  
 Fax: 516-694-6715

**INTERNATIONAL**  
 Tel: 805-778-9229  
 Fax: 805-778-1980

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 Tel: 603-888-3975  
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[www.aeroflex.com](http://www.aeroflex.com) [info-ams@eroflex.com](mailto:info-ams@eroflex.com)

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