

Aeroflex Colorado Springs Application Note

Interfacing the 3.3V RadHard Eclipse FPGA with 5V devices

1.0) Introduction

With the proliferation of multiple process geometries (i.e., 0.6 μ m, 0.35 μ m, 0.25 μ m, and 0.18 μ m, etc.), electronic systems find an ever-increasing need to interface semiconductor devices that have incompatible voltages. When these systems require a combination of 3V and 5V devices, for example, designers need consider to reliability, signal integrity, power, performance and board space. Typically, devices with different I/O voltages cannot be directly interfaced without external signal conditioning. This document will describe several ways to condition incompatible signal voltages while addressing the design considerations mentioned above. Depending upon the specific application requirements, one or more of the following approaches may be applicable to your design.

2.0) Series Current Limit

Some vendors handle this issue using a simple series resistor. However, there are many pitfalls with this approach, including increased power consumption, slower performance and reduced reliability. When a 5V output drives a 3V input through a series resistor, current density and long term reliability of the 3V device becomes an issue. Depending upon the current limiting capability of the series resistor (e.g. 50 Ω), the 3V device could see its inputs sinking up to 36mA of current. When these conditions exist, metal migration becomes a major concern. To combat the metal migration concern and minimize the amount of current dumped onto the 3V power supply, a large series resistance (e.g. 1k Ω) should be used. Consequently, the large series resistance severely slows down the signal and reduces noise immunity on the net. For these reasons, Aeroflex does not recommend this approach.

3.0) 5V and 3V Interface using Resistive Divider Networks

The Aeroflex RadHard Eclipse FPGA can be driven by a 5V device using a resistive voltage divider. A voltage divider network will limit the input voltage while allowing the current to flow to ground rather than through the ESD protection circuitry of the FPGA. Although the resistive divider, like the series current limit alternative, suffers from an increased DC leakage current while the input is high, it does not suffer from reliability degradation like the series resistance approach. The voltage divider resistance values can be determined using equations 1 through 5 in conjunction with Figures 1 and 2 below:

$$(eq1) \quad k = R_3 / (R_1 + R_2 + R_3)$$

$$(eq2) \quad R_{tot} = R_1 + R_2 + R_3$$

$$(eq3) \quad I_{leak} = V_{drive} / R_{tot}$$

$$(eq4) \quad V_2 = k * V_{drive}$$

$$(eq5) \quad Z_0 = R_1; \text{ where } R_1 = R_{series} + R_{driver}$$

The series resistances should be selected to match the characteristic impedance (Z_0) of the interconnecting trace. Smaller series resistance values will result in a larger leakage current when the net is driven high because a proportionately smaller resistance would have been selected for R_3 to ensure proper voltage division and, by necessity, reducing the total impedance R_{tot} from the 5V driver to ground. However, the smaller series resistances will facilitate a higher signal rate on the net. Conversely, choosing larger series resistors reduces power consumption, but increase the signal propagation delay. The designer will have to decide what resistive values are best suited toward satisfying the design requirements for the particular application.

Furthermore, the resistors should be placed as close as possible to their corresponding devices. This creates a “lumped” impedance at each driver and receiver, thus reducing noise and signal reflections at driver outputs and receiver inputs. When implementing a multi-drop or bussed architecture, it is best to have a “star topology”, where all stubs are equal length and the fanout occurs at one point located at the exact middle of the network.

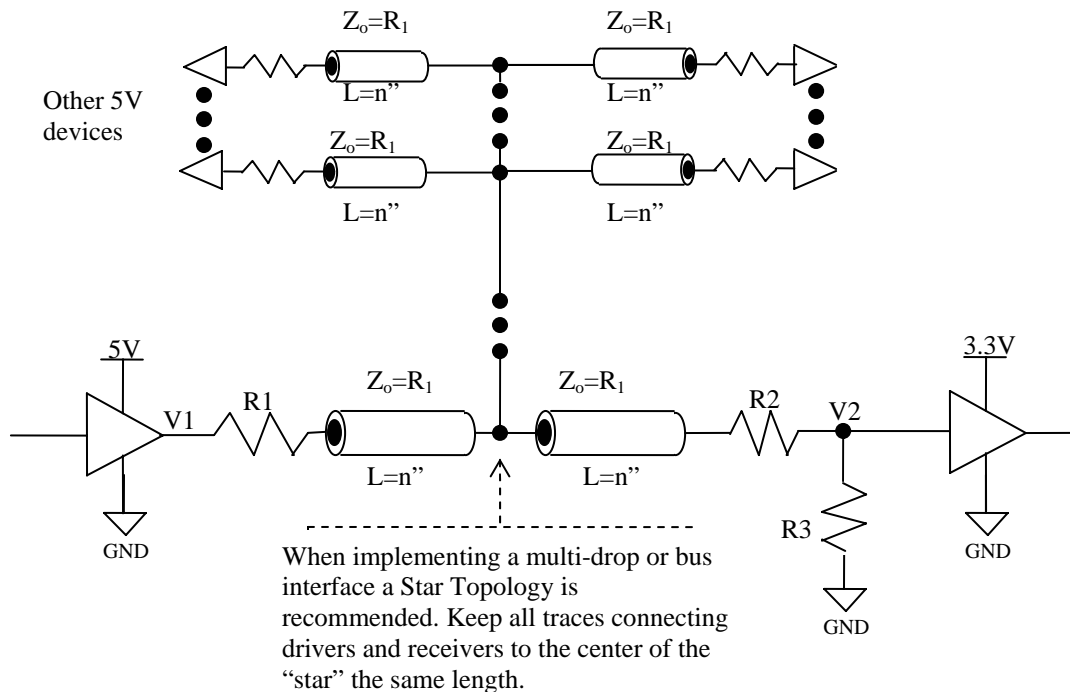


Figure 1: Input Only Interface

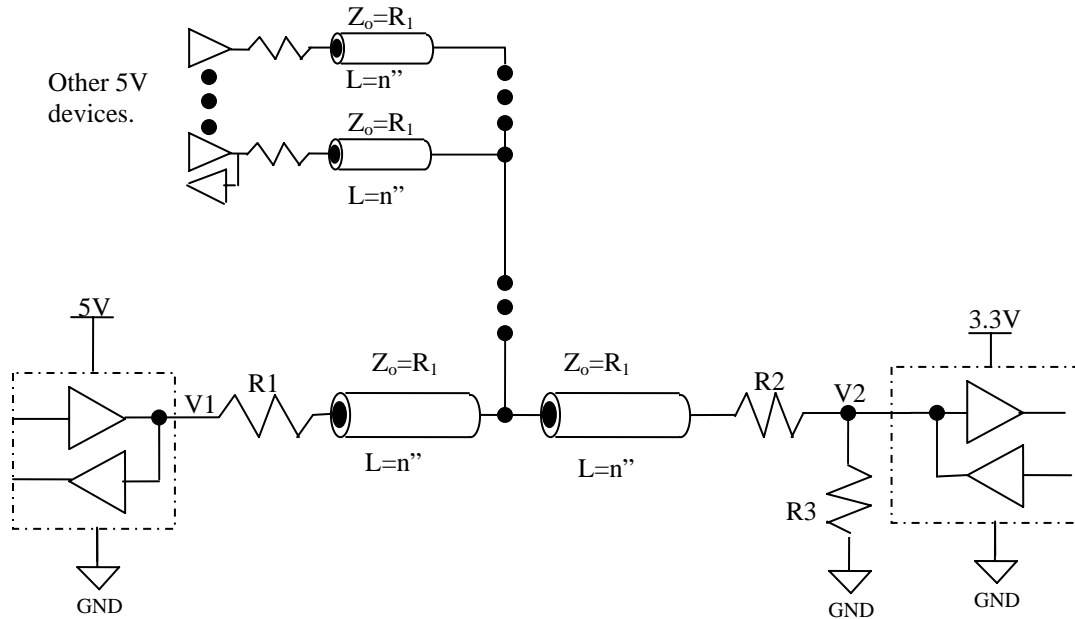


Figure 2: Bi-Directional Interface

For the case of a bi-directional bus where the 3V device drives the 5V inputs on the network, the current load of all devices on the net should be kept sufficiently low to ensure the 3V driver attains a high enough voltage to satisfy the minimum high level voltage required by the 5V inputs. Note, this option is only viable for a 3V output driving TTL compatible inputs. A 3V driver cannot drive 5V CMOS voltage levels. If the user's application does not permit the additional leakage current, or is unable to ensure a sufficiently small load for the 3V driver, Aeroflex recommends the use of a level translating bus transceiver like the UT54ACS164245SE.

4.0) UT54ACS164245SE Voltage Translating Bus Transceiver **(www.aeroflex.com/radhard)**

When room is available, The Aeroflex UT54ACS164245SE voltage translating transceiver is ideally suited for applications where a 5V device needs to interface with a 3V device like the Aeroflex RadHard Eclipse. Although the UT54ACS164245SE requires more area than the resistor divider described in section 3.0, it is the most reliable and lowest risk means to implement a mixed-voltage interface. This solution guarantees a low output-to-output skew and consumes less power than a large array of voltage dividers. Furthermore, the UT54ACS164245SE guarantees V_{IH} levels for both CMOS and TTL signaling for both 3V and 5V interfaces. It also provides additional signal buffering to drive large nets and heavy loads while providing tri-state and direction control for the designer.

Conclusion

Aeroflex Colorado Springs recommends addressing this 5V/3V interface using voltage divider networks or using the Aeroflex UT54ACS164245SE voltage transceiver as described.