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APPLICATION NOTE #107

CT2525/6/7 Series
CT7005/6 Series

OVERVIEW OF SOME TYPICAL RT/BC TO SUBSYSTEM IMPLEMENTATIONS

PART 1: HARDWARE REQUIREMENTS

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GENERAL

The CT252X Series of hybrids provide a complete one package interface between the MIL-STD-1553 bus and all microprocessor systems. The microcircuit reduces the military interface from three hybrids in Aeroflex's previous product line down to a single component less than 2½ inches square.

All the necessary electronics to implement either a Remote Terminal (RT) or a Bus Controller (BC) are contained in the hybrid package. The major sections of the hybrid are the µP interface (with an internal block-arbitrated RAM), a dual transceiver, and the 1553 protocol handler. The CM252X µP interface is a functional superset of the CT1800 and is downwardly compatible with the existing base of CT1800 designs. The transceiver section is available in three configurations, Table 1 lists the power supply and bus transformer requirements. The protocol handler is based on the CT1612, which fully supports all MIL-STD-1553B commands and mode codes. All circuitry (excluding transceiver drivers) are CMOS, which results in very low power requirements.

The hybrid is also available as the CT2528, which is a complete BC/RT without the internal transceivers. This enables the end user to use a different type of transceiver, such as a fiber optic transmitter/receiver for MIL-STD-1773 applications.

SUBSYSTEM INTERFACE

A typical CM252X to subsystem configuration is shown in Figure 1. The schematic diagram will also work for the CT2525 and CT2526, with the only differences being the power supply connections and transformer selection (See CT2525/6/7/8 Data Sheet). Some of the more noteworthy features of the hybrid are as follows:

- Since all sub-address data and operations of the BC/RT are accessed using the four address inputs (A0-A3), the subsystem only has to give up 16 address locations in its memory map. This is in direct contrast to some BC/RT's that use a complex stack or DMA architecture, which sometimes forces the subsystem to give up as much as 8K of address locations in the memory map.
- Interfacing to the subsystem data bus is simplified through the use of internal tri-stated data buffers. The BC/RT data bus can be configured for 8 or 16 bit operation through the use of the M16/8 signal (pin 28) on the hybrid.
- Simple control signals are utilized by the hybrid. They consist of four address inputs (A0-A3), a device-select input ($\overline{DS}$), a read strobe ($\overline{RD}$), a write strobe ($\overline{WR}$), and several interrupts (optional use). All of these signals are normally provided by any microprocessor.

The above features enables the BC/RT to appear as nothing more than a simple I/O peripheral or a small block of memory on the subsystem data bus. The CT252X will easily interface with almost any microprocessor, from a Z80 up to a 68040.

(Continued on page 4)

Table 1

HYBRID PART NUMBER:	CT2525	CT2526	CT2527 *
POWER SUPPLY REQUIREMENTS:	+15,-15,+5	+12,-12,+5	+ 5
TECHNITROL TRANSFORMER:	Ql553-2	Ql553-1	Ql553-35

* Applies to CT7005 and CT7006

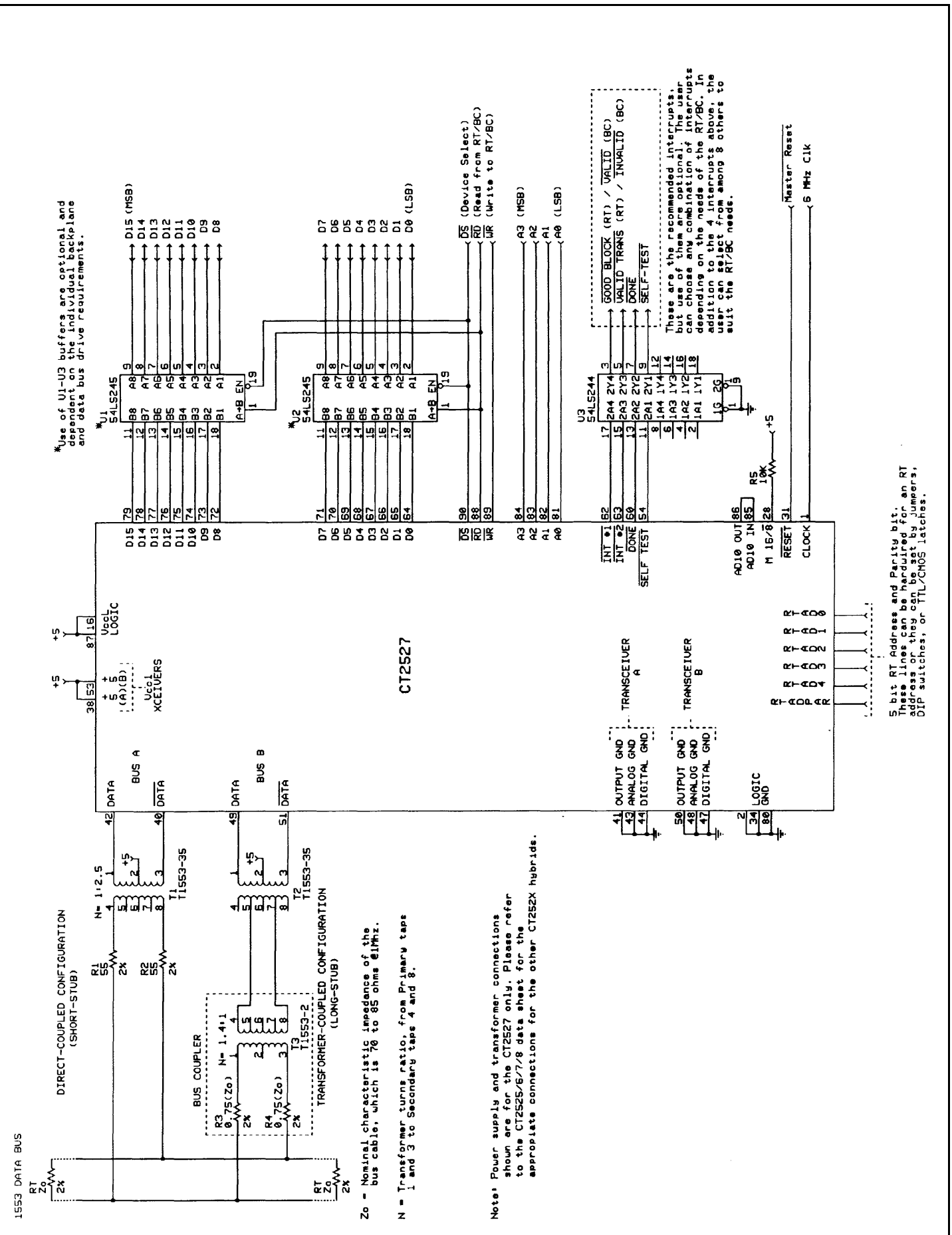

1553 DATA BUS
RT Zo 2%
DIRECT-COUPLED CONFIGURATION (SHORT-STUB)
BUS COUPLER
TRANSFORMER-COUPLED CONFIGURATION (LONG-STUB)
R1 55 2%
R2 55 2%
R3 0.75(Zo) 2%
R4 0.75(Zo) 2%
N= 1:2.5
N= 1.4:1
T1 T1553-35
T2 T1553-35
T3 T1553-2
Zo = Nominal characteristic impedance of the bus cable, which is 70 to 85 ohms @1Mhz.
N = Transformer turns ratio, from Primary taps 1 and 3 to Secondary taps 4 and 8.
Note: Power supply and transformer connections shown are for the CT2527 only. Please refer to the CT2525/6/7/8 data sheet for the approprate connections for the other CT252X hybrids.
*Use of U1-U3 buffers are optional and dependent on the individual backplane and data bus drive requirements.
U1 54LS245
U2 54LS245
U3 54LS244
A+B EN
+5 Vcc1 LOGIC
+5 Vcc1 XCEIVERS
BUS A
BUS B
DATA
CT2527
TRANSCEIVER A
TRANSCEIVER B
OUTPUT GND
ANALOG GND
DIGITAL GND
LOGIC GND
D15 (MSB)
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0 (LSB)
DS (Device Select)
RD (Read from RT/BC)
WR (Write to RT/BC)
A3 (MSB)
A2
A1
A0 (LSB)
INT #1
INT #2
DONE
SELF TEST
GOOD BLOCK (RT) / VALID (BC)
VALID TRANS (RT) / INVALID (BC)
DONE
SELF-TEST
These are the recommended interrupts, but use of them are optional. The user can choose any combination of interrupts depending on the needs of the RT/BC. In addition to the 4 interrupts above, the user can select from among 8 others to suit the RT/BC needs.
AD10 OUT
AD10 IN
M 16/8
R5 10K
RESET
CLOCK
Master Reset
6 MHz Clk
RT ADDR 4
RT ADDR 3
RT ADDR 2
RT ADDR 1
RT ADDR 0
RT PARITY
5 bit RT Address and Parity bit. These lines can be hardwired for an RT address or they can be set by jumpers, DIP switches, or TTL/CMOS latches.

Figure 1

HARDWARE REQUIREMENTS

A minimal amount of external circuitry is needed to complete the 1553 interface because of the high degree of integration in the CT252X hybrids. The following text shall discuss the basics in completing a RT/BC black box. The concepts presented here are not meant to be definitive, the designer is encouraged to elaborate on them to implement his/her particular application.

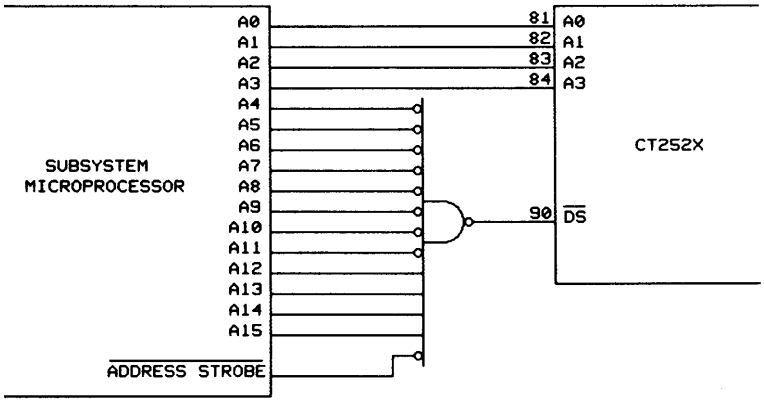
1553 BUS: On the 1553 bus side of the RT/BC the designer has to choose the appropriate transformer (See Table 1) and isolation resistors according to the CT252X hybrid that is being utilized. The schematic in Figure 1 shows connections for both direct-coupled (short stub) and transformer-coupled (long stub) configurations. This completes the hardware requirements for the 1553 bus interface.

DATA BUS (D0-DI5): On the subsystem side some additional hardware may be needed to complete the interface. If the RT/BC must interface to the µP/subsystem through a backplane or extended wiring, then 54LS TTL buffers should be used to increase the hybrid's current drive capability. This is illustrated in Figure 1.

ADDRESS LINES (A0-A3): In most cases the RT/BC will coexist with RAM and other I/O devices on the subsystem data and address lines. Though the CT252X requires only 16 address locations, they must be uniquely qualified so that there is no contention with other devices on the data bus. Figure 2 illustrates a typical µP that has a maximum address space of 64K. In this example the BC/RT is being assigned addresses F000-F00FH in the memory map. The output of the NAND-gate decoder will go low when an address in the range of F000-F00FH is valid, this will qualify the master enable input (DS) of the CT252X. The address decoder function can be designed using discrete logic, or implemented in a PAL or PLD along with other discrete logic that might be on the system board.

READ and WRITE LINES: Many microprocessors do not provide the separate read and write signals that the CT252X utilizes, instead they provide a single Read/ Write output and a Data or I/O strobe to qualify it. The 68000 family of microprocessors is an example of this type of device; Figure 3 shows a simple circuit that can be used to interface it to the $\overline{RD}$ and $\overline{WR}$ lines of the C252X. The microprocessor's $\overline{DATA\ STROBE}$ output is used to format it's R/W output into two discrete active low

Figure 2 Address Decoder Logic



pulses for the $\overline{RD}$ and $\overline{WR}$ inputs of the RT/BC subsystem interface. Using the $\overline{DATA\ STROBE}$ signal ensures that the µP data bus is ready to receive or transmit information.

RT ADDRESS LINES (RTAD0-RTAD4): These inputs are used to set the 1553 Remote Terminal Address of the C252X. The RTADPAR input is used in conjunction with the address lines to set the parity of the RT address. The RT address parity must be odd at all times, even if the C7252X is in the BC mode. Odd parity means that the number of logic 1's on the RT Address and Parity inputs must equal an odd number (1, 3, or 5). Table 2 shows a few examples of RT addresses with odd parity set.

Table 2

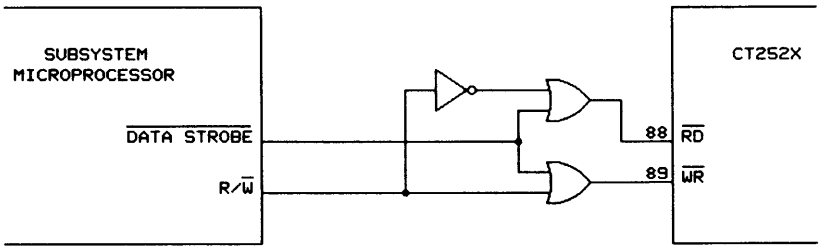
DECIMAL	ADDRESS BITS					PARITY BIT	COMMENTS
	4	3	2	1	0		
0	0	0	0	0	0	1	VALID
22	1	0	1	1	0	0	VALID
29	1	1	1	0	1	1	VALID
8	0	1	0	0	0	1	NOT VALID
8	0	1	0	0	0	0	VALID

It should be noted that each RT Address input has an internal pull-up to the +5V supply, this gives the ability to program the inputs using either DIP switches or jumpers. An advanced feature would be to connect the RT Address inputs to the output of a CMOS or TTL octal D-type latch. The input to the latch would be connected to the µP data bus and the latch would then be addressed as an I/O port or as a single address in the memory map. This would give the ability to set or change the RT address through software control.

INTERRUPT LINES: The CT252X has 12 discrete output signals for the purpose of providing transfer and status information of the 1553 bus to the subsystem. By utilizing the interrupts, the designer no longer has to dedicate a separate microprocessor to supervise transfers over the 1553 bus. The same µP that is used to process subsystem information (i.e. fuel gauge data, altimeter readings, radar info, etc.) can also be used to transfer information to and from the 1553 bus, this is because the architecture of the CT252X does not require the subsystem to continuously poll the RT/BC interface of the hybrid.

The majority of the CT252X interrupts are active low outputs with a nominal pulse width of 160ns. These outputs are adequate for interfacing to discrete logic and state sequencer type designs. Some additional logic may be necessary when interfacing to a µP, this is because most microprocessors require that an interrupt be present for at least 2 to 5 clock cycles. After the number of required clock cycles has passed, the µP will usually generate an output known as Interrupt Acknowledge

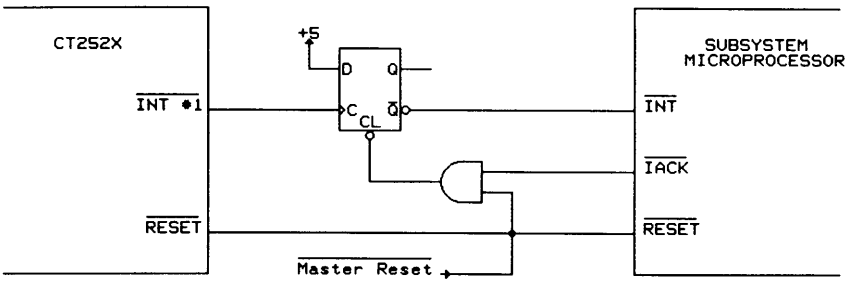
Figure 3 Read/Write Interfacing for a Typical Motorola Processor



($\overline{\text{IACK}}$), indicating that the pending interrupt has been recognized.

Figure 4 shows a simple circuit that will detect an interrupt and hold it until the µP acknowledges its presence. It should be noted that the figure shown is an oversimplification

Figure 4 Interrupt Control Logic



SUMMARY

This paper has attempted to answer the most commonly asked questions concerning the use of the CT252X series of hybrids. Forthcoming application notes will address additional hardware concerns and software methodology. Information on the CT252X series, or any other 1553 data bus product, can be obtained by calling the Applications Dept. at (516) 752-2484.