

## UT54LVDS217 Transmitter Pulse Position (TPPosN) and UT54LVDS218 Receiver Strobe Position (RSPosN) Estimate Over Frequency

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC
3.0V SERIALIZER	UT54LVDS217	5962-01534	01, 02	WD11, WD13
3.0V DESERIALIZER	UT54LVDS218	5962-01535	01, 02	WD12, WD14

### 1.0 Overview

The UT54LVDS217 Serializer converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock (Tx CLK IN) 21 bits of input data are sampled and transmitted. The UT54LVDS218 Deserializer converts the three LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 75MHz, 21 bits of TTL data are transmitted at a rate of 525Mbps per LVDS data channel. Using a 75MHz clock, the data throughput is 1.575 Gbps.

This application note provides estimates of Transmitter Strobe Position, TPosN, and Receiver Strobe Position, RSPosN, for 25 to 75 MHz. TPosN and RSPosN values for various frequencies are necessary for estimating system timing requirements and calculating Receiver Input Skew Margin, RSKM. See APP-LVDS-012 for an example of how to calculate RSKM.

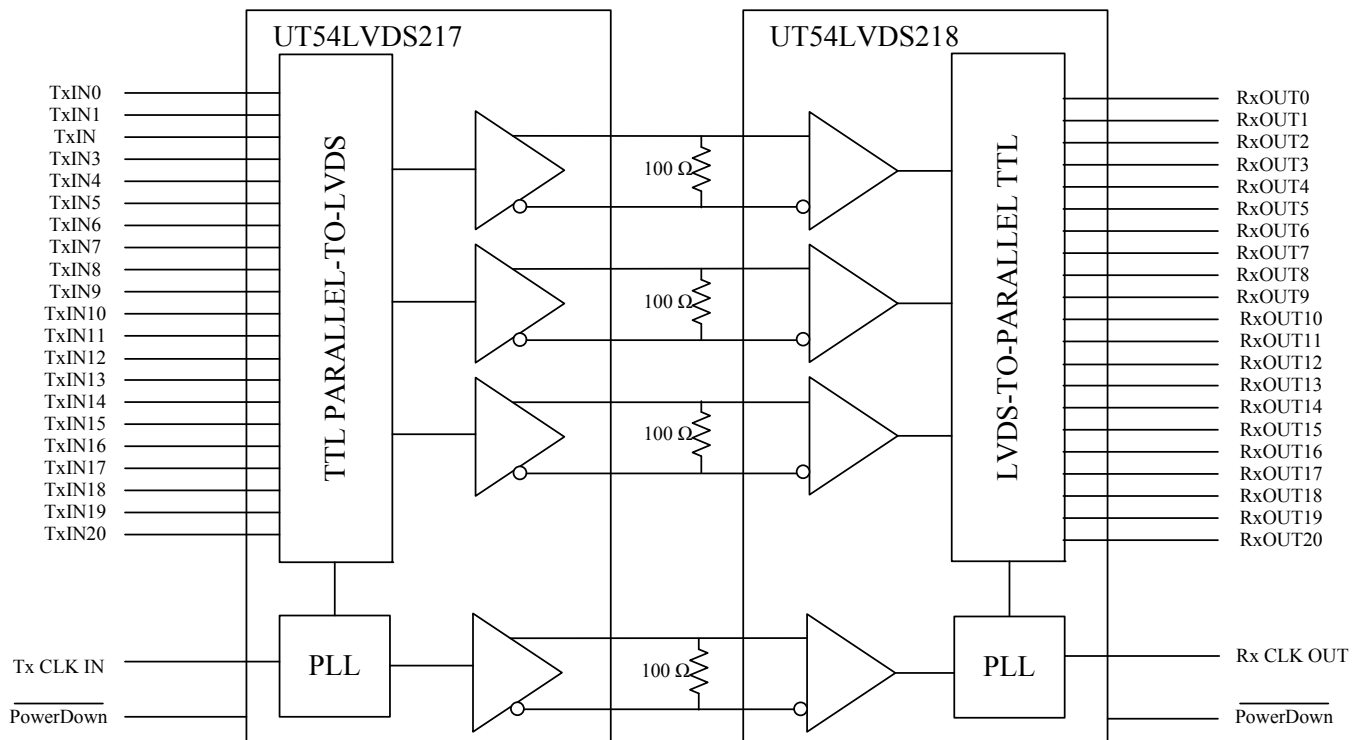


Figure 1. Standard UT54LVDS217 and UT54LVDS218 Configuration

## 2.0 TPPosN and RSPosN Data

The UT54LVDS217 Serializer, 217, and the UT54LVDS218 Deserializer, 218, are ideal for applications where a high speed, low power, and low harness mass is required. The recommended operating frequencies for these devices are 25MHz to 75MHz. Both the 217 and 218 datasheets and corresponding SMDs contain AC Switching Characteristics for 75MHz only. 75MHz operation presents the worst case, or narrowest pulse and strobe position windows.

Many system designers require an estimate of TPosN and RSPosN performance at frequencies less than 75MHz. Figures 2 – 15 are intended to provide estimates of TPosN and RSPosN. Using the data contained in Tables 2, 3, 4, and 5 trend lines can be extrapolated from the 25MHz and 75MHz data. These graphs which allow a system designer to estimate how the min/max TPosN and min/max RSPosN shift with respect to the input clock frequency. Data in Tables 2 - 7 is NOT GUARANTEED

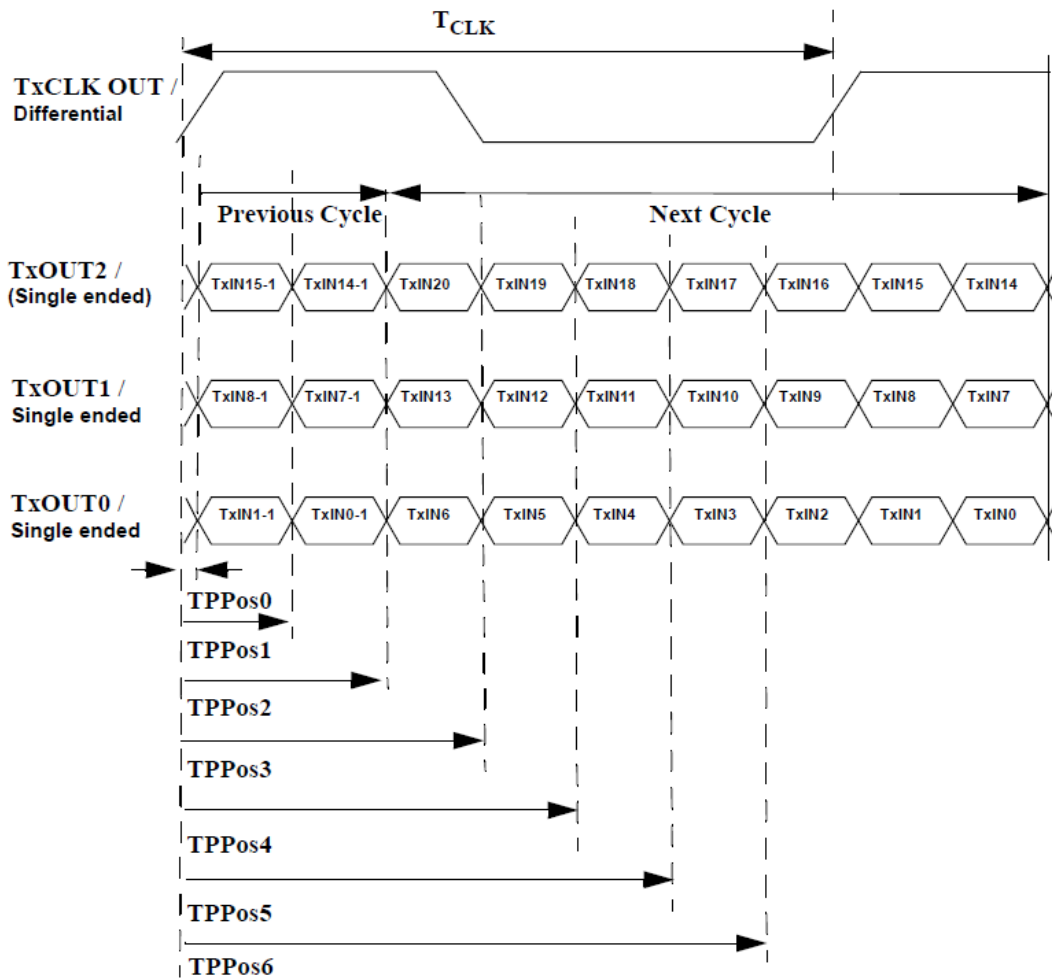


Figure 2. UT54LVDS217 TPosN Timing Diagram from Datasheet

Table 2. UT54LVDS217 the Transmitter Output Pulse Positions at 25MHz

**UT54LVDS217 TRANSMITTER SWITCHING CHARACTERISTICS**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>
TPPos0	Transmitter Output Pulse Position for Bit 0	-0.05	0.08	ns
TPPos1	Transmitter Output Pulse Position for Bit 1 f=25MHz	5.67	5.84	ns
TPPos2	Transmitter Output Pulse Position for Bit 2 f=25MHz	11.37	11.57	ns
TPPos3	Transmitter Output Pulse Position for Bit 3 f=25MHz	17.05	17.25	ns
TPPos4	Transmitter Output Pulse Position for Bit 4 f=25MHz	22.81	23.03	ns
TPPos5	Transmitter Output Pulse Position for Bit 5 f=25MHz	28.49	28.73	ns
TPPos6	Transmitter Output Pulse Position for Bit 6 f=25MHz	34.18	34.49	ns

Table 3. UT54LVDS217 the Transmitter Output Pulse Positions at 50MHz

**UT54LVDS217 TRANSMITTER SWITCHING CHARACTERISTICS**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>
TPPos0	Transmitter Output Pulse Position for Bit 0	-0.13	0.02	ns
TPPos1	Transmitter Output Pulse Position for Bit 1 f=50MHz	3.04	3.23	ns
TPPos2	Transmitter Output Pulse Position for Bit 2 f=50MHz	5.67	5.82	ns
TPPos3	Transmitter Output Pulse Position for Bit 3 f=50MHz	8.52	8.72	ns
TPPos4	Transmitter Output Pulse Position for Bit 4 f=50MHz	11.56	11.73	ns
TPPos5	Transmitter Output Pulse Position for Bit 5 f=50MHz	14.19	14.34	ns
TPPos6	Transmitter Output Pulse Position for Bit 6 f=50MHz	17.30	17.47	ns

Table 4. UT54LVDS217 the Transmitter Output Pulse Positions at 75MHz (From device datasheet)

**UT54LVDS217 TRANSMITTER SWITCHING CHARACTERISTICS**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>
TPPos0	Transmitter Output Pulse Position for Bit 0	-0.18	0.27	ns
TPPos1	Transmitter Output Pulse Position for Bit 1 f=75MHz	1.72	2.17	ns
TPPos2	Transmitter Output Pulse Position for Bit 2 f=75MHz	3.63	4.08	ns
TPPos3	Transmitter Output Pulse Position for Bit 3 f=75MHz	5.53	5.98	ns
TPPos4	Transmitter Output Pulse Position for Bit 4 f=75MHz	7.44	7.89	ns
TPPos5	Transmitter Output Pulse Position for Bit 5 f=75MHz	9.34	9.79	ns
TPPos6	Transmitter Output Pulse Position for Bit 6 f=75MHz	11.25	11.7	ns

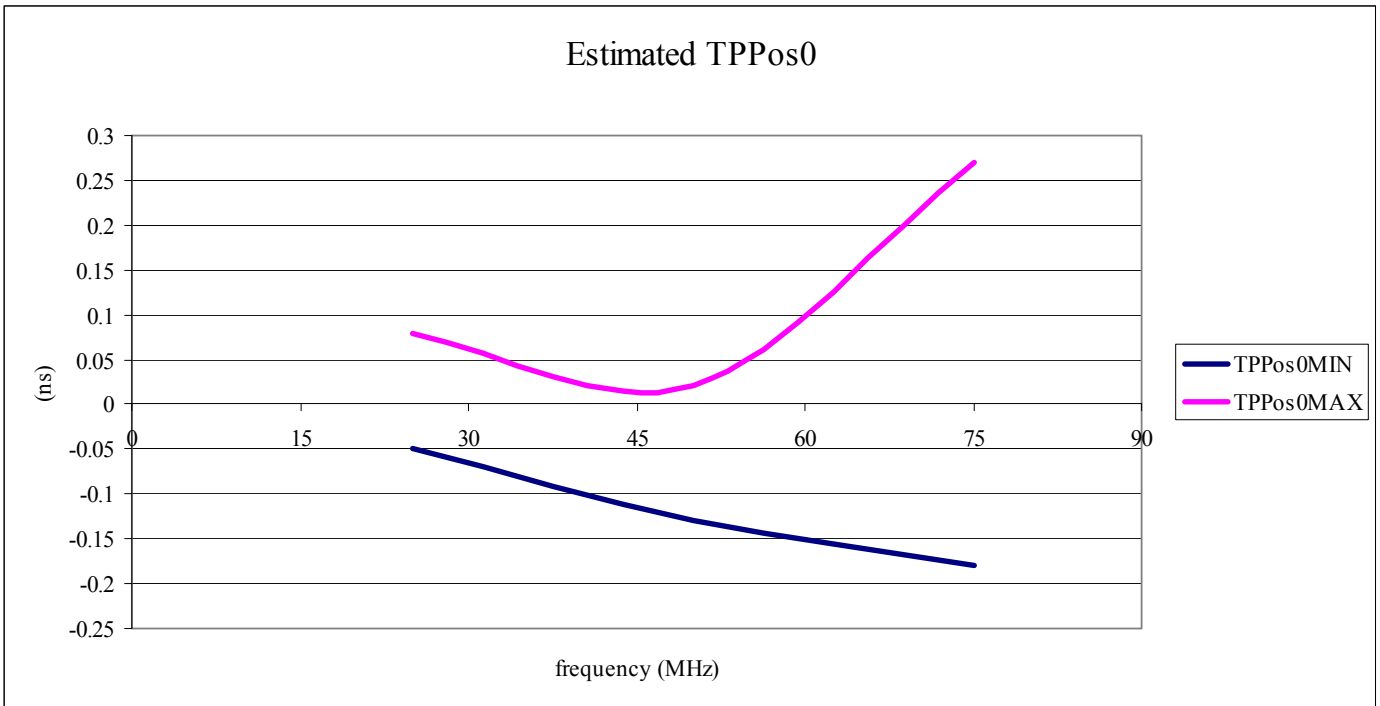


Figure 3. Estimated TPPos0 over frequency

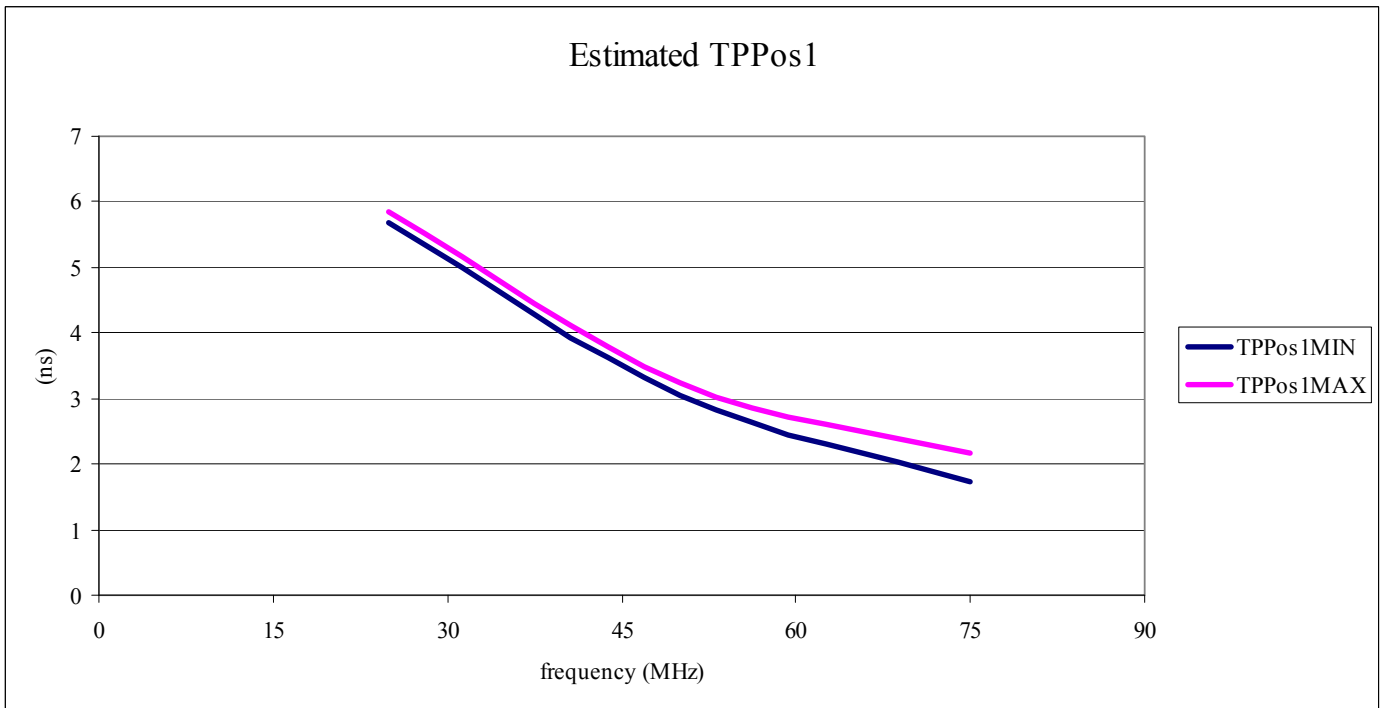


Figure 4. Estimated TPPos1 over frequency

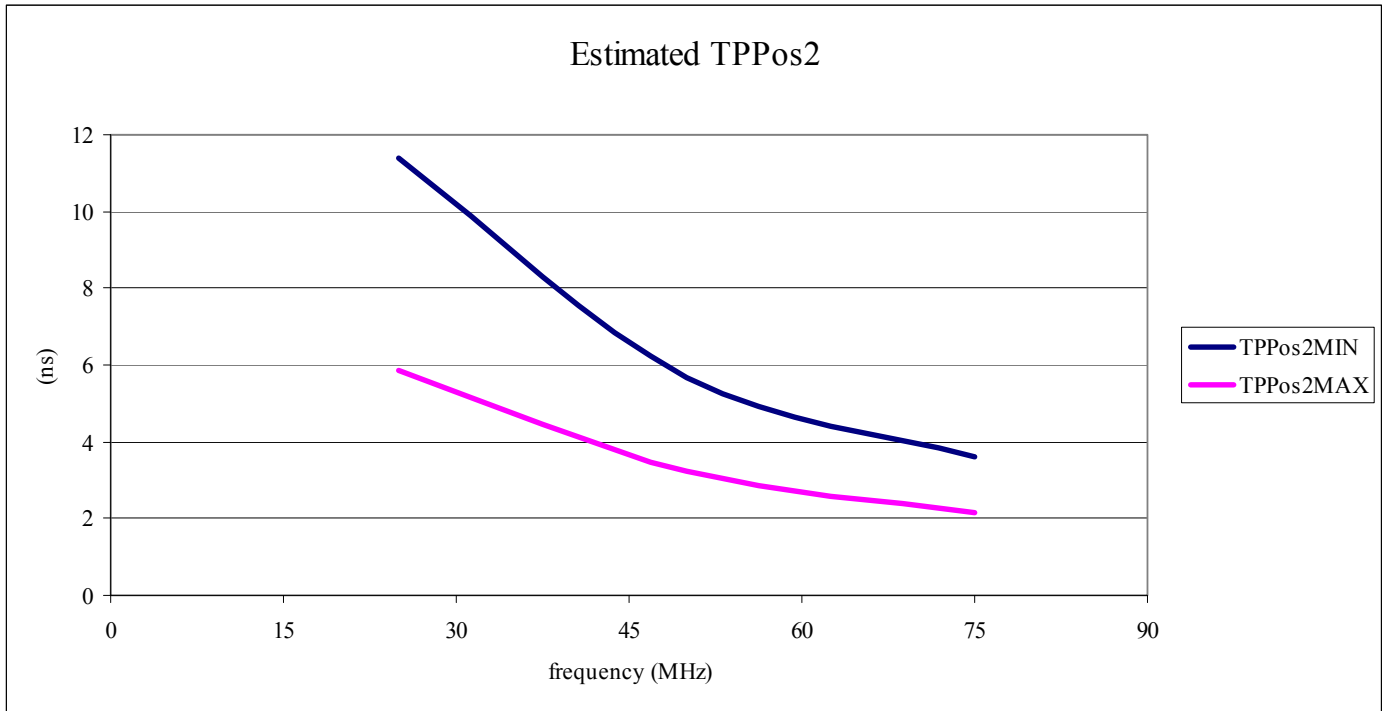


Figure 4. Estimated TPPos2 over frequency

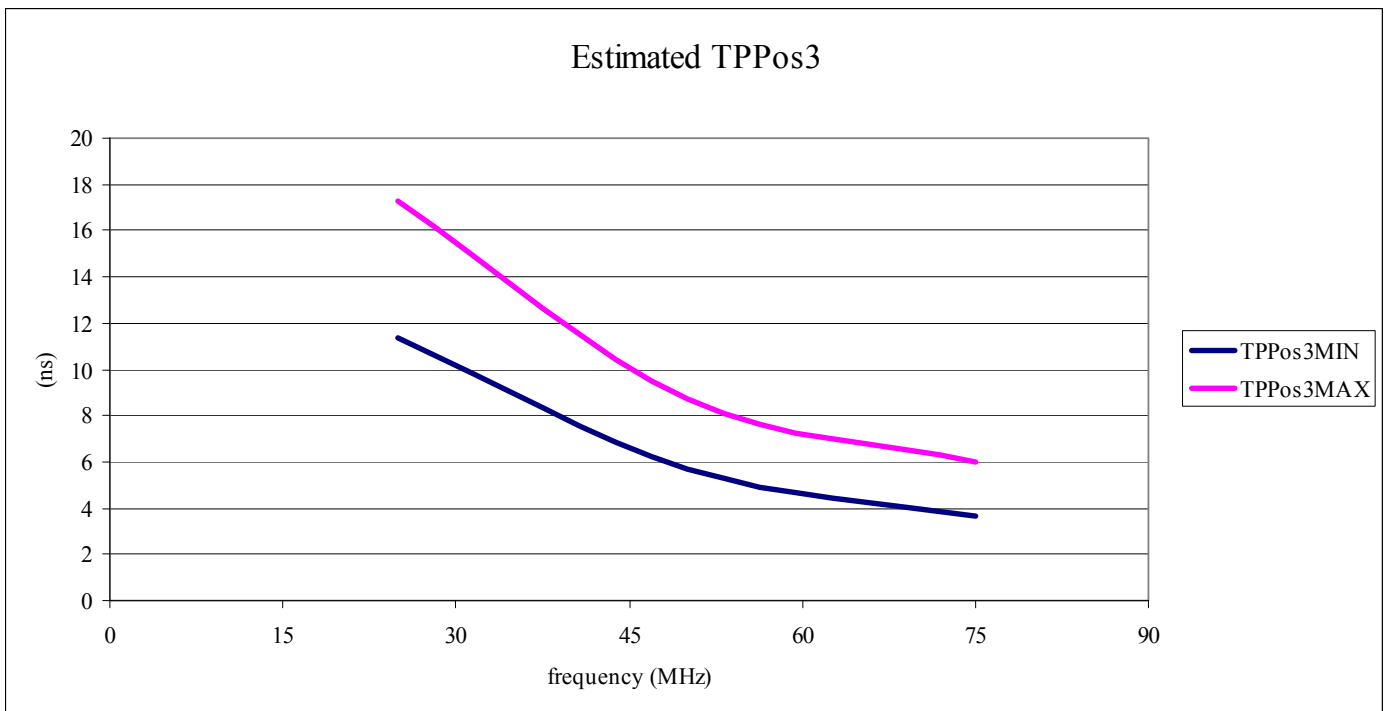


Figure 6. Estimated TPPos3 over frequency

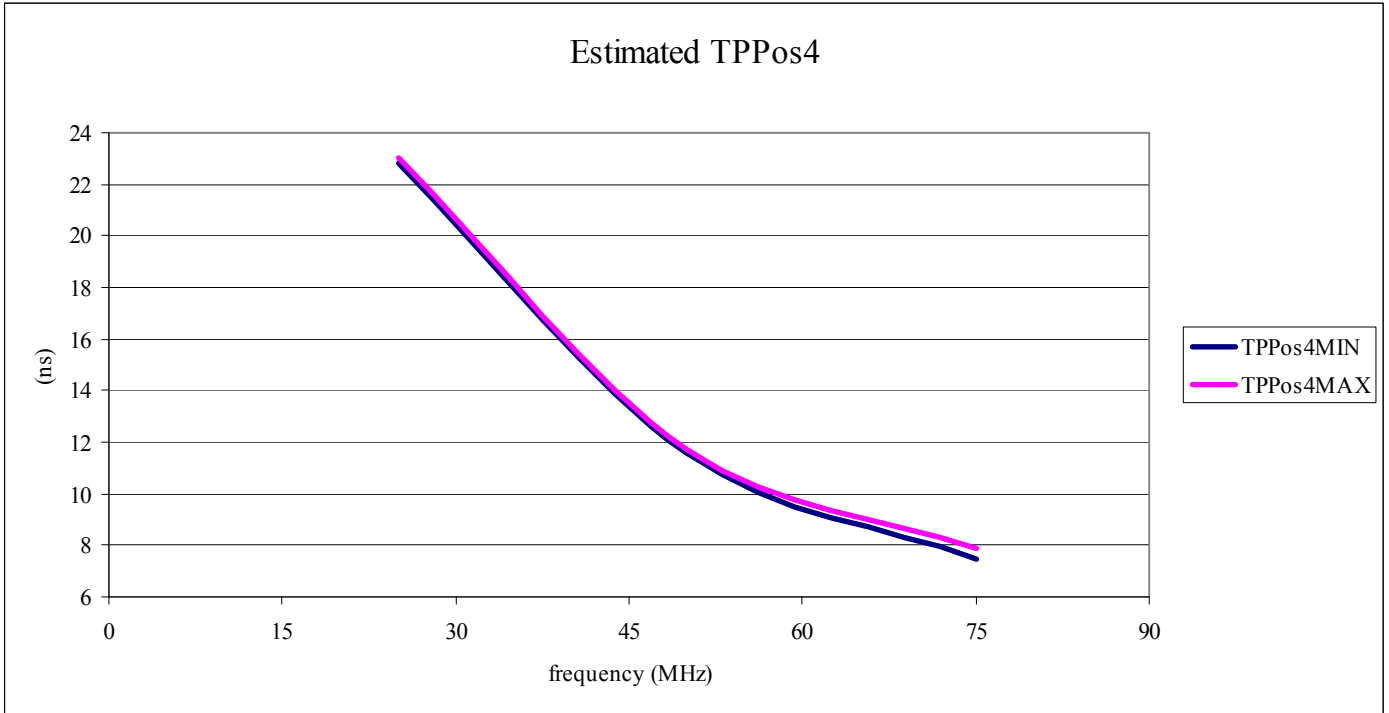


Figure 7. Estimated TPPos4 over frequency

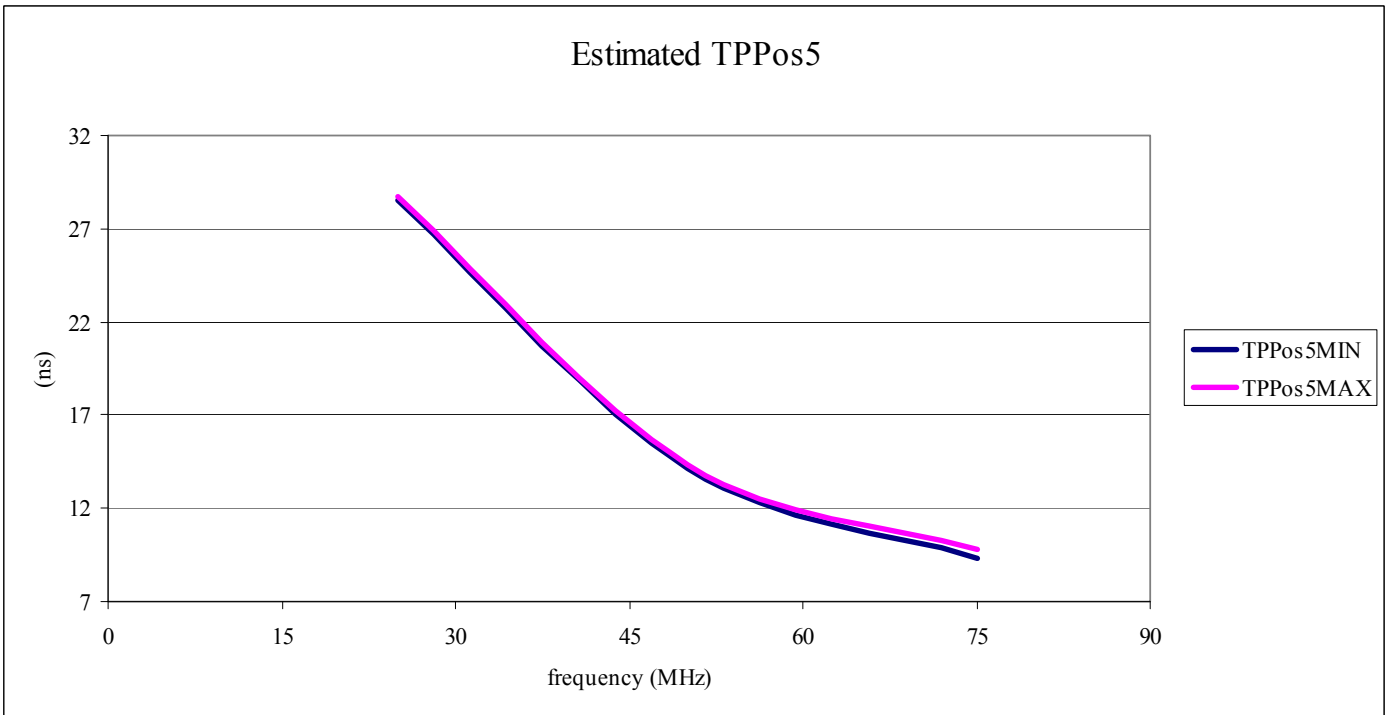


Figure 8. Estimated TPPos5 over frequency

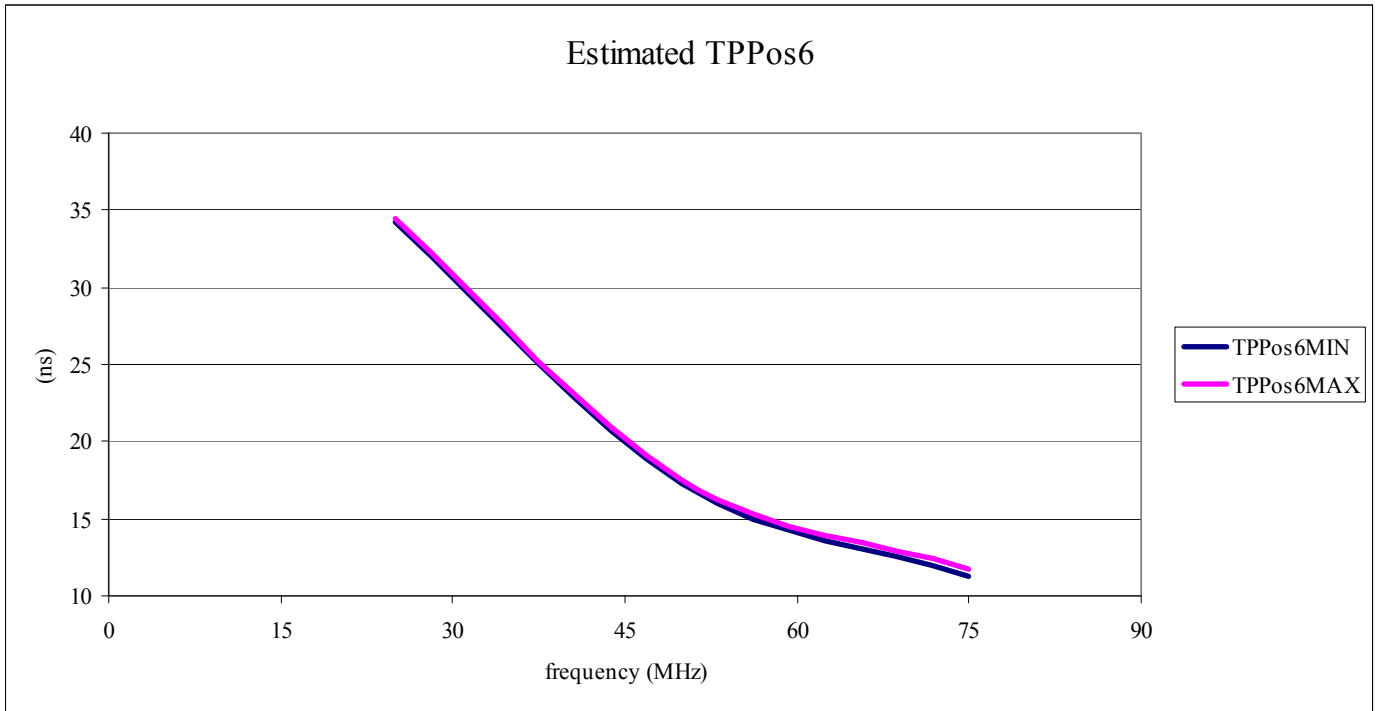


Figure 9. Estimated TPPos6 over frequency

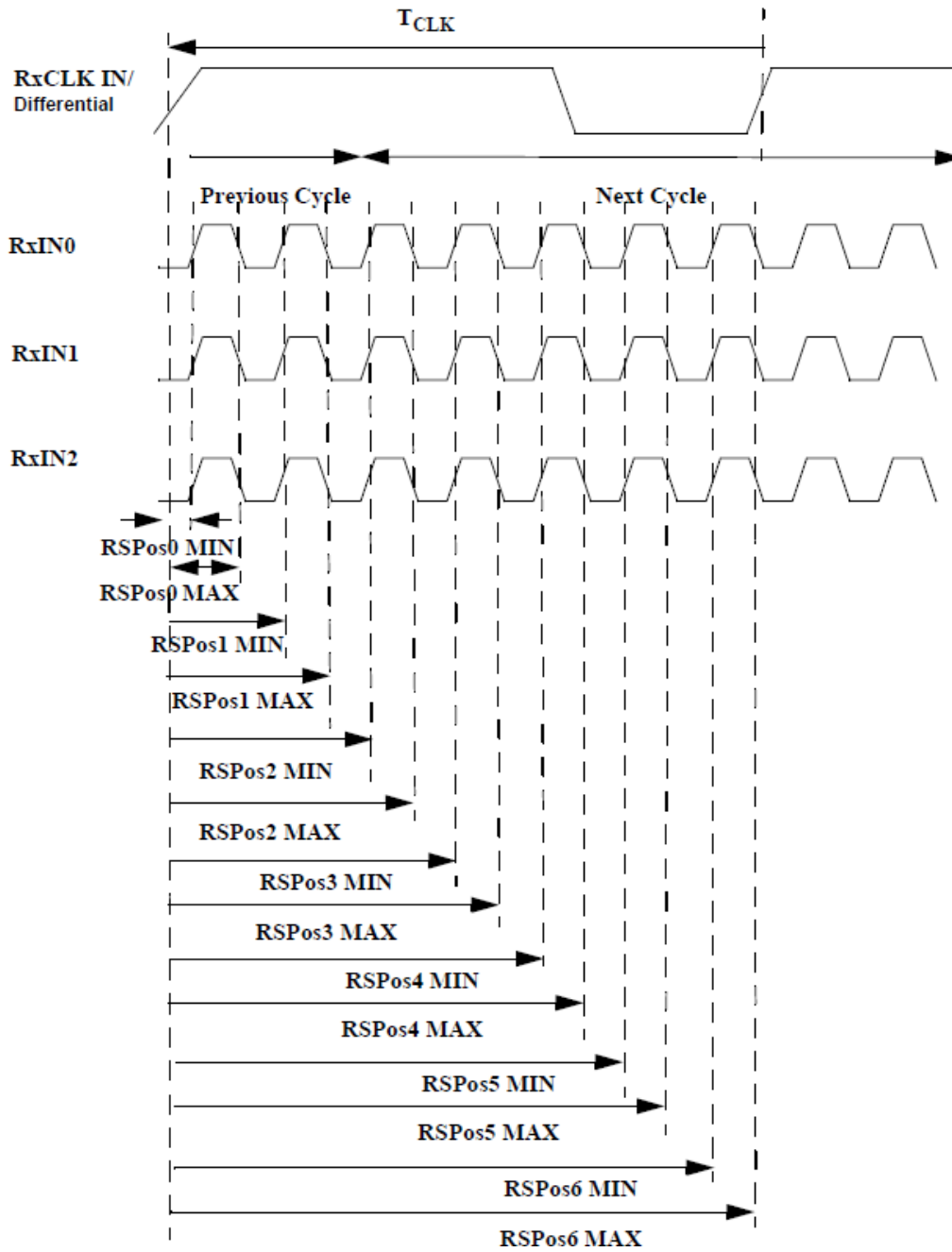


Figure 10. UT54LVDS218 RSPosN Timing Diagram from Datasheet

Table 5. UT54LVDS218 the Receiver Input Strobe Positions at 25MHz

**UT54LVDS218 RECEIVER SWITCHING CHARACTERISTICS**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>
RSPos0	Receiver Input Strobe Position for Bit 0	1.72	2.77	ns
RSPos1	Receiver Input Strobe Position for Bit 1 f=25MHz	7.43	8.49	ns
RSPos2	Receiver Input Strobe Position for Bit 2 f=25MHz	13.15	14.22	ns
RSPos3	Receiver Input Strobe Position for Bit 3 f=25MHz	18.88	19.93	ns
RSPos4	Receiver Input Strobe Position for Bit 4 f=25MHz	24.58	25.64	ns
RSPos5	Receiver Input Strobe Position for Bit 5 f=25MHz	30.28	31.35	ns
RSPos6	Receiver Input Strobe Position for Bit 6 f=25MHz	36.00	37.08	ns

Table 6. UT54LVDS218 the Receiver Input Strobe Positions at 50MHz

**UT54LVDS218 RECEIVER SWITCHING CHARACTERISTICS**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>
RSPos0	Receiver Input Strobe Position for Bit 0	0.88	2.05	ns
RSPos1	Receiver Input Strobe Position for Bit 1 f=50MHz	3.74	4.90	ns
RSPos2	Receiver Input Strobe Position for Bit 2 f=50MHz	6.60	7.77	ns
RSPos3	Receiver Input Strobe Position for Bit 3 f=50MHz	9.46	10.62	ns
RSPos4	Receiver Input Strobe Position for Bit 4 f=50MHz	12.31	13.47	ns
RSPos5	Receiver Input Strobe Position for Bit 5 f=50MHz	15.17	16.34	ns
RSPos6	Receiver Input Strobe Position for Bit 6 f=50MHz	18.03	19.19	ns

Table 7. UT54LVDS218 the Receiver Input Strobe Positions at 75MHz (From device datasheet)

**UT54LVDS218 RECEIVER SWITCHING CHARACTERISTICS**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>
RSPos0	Receiver Input Strobe Position for Bit 0	0.5	1.24	ns
RSPos1	Receiver Input Strobe Position for Bit 1 f=75MHz	2.41	3.15	ns
RSPos2	Receiver Input Strobe Position for Bit 2 f=75MHz	4.31	5.05	ns
RSPos3	Receiver Input Strobe Position for Bit 3 f=75MHz	6.22	6.96	ns
RSPos4	Receiver Input Strobe Position for Bit 4 f=75MHz	8.12	8.86	ns
RSPos5	Receiver Input Strobe Position for Bit 5 f=75MHz	10.03	10.77	ns
RSPos6	Receiver Input Strobe Position for Bit 6 f=75MHz	11.93	12.67	ns

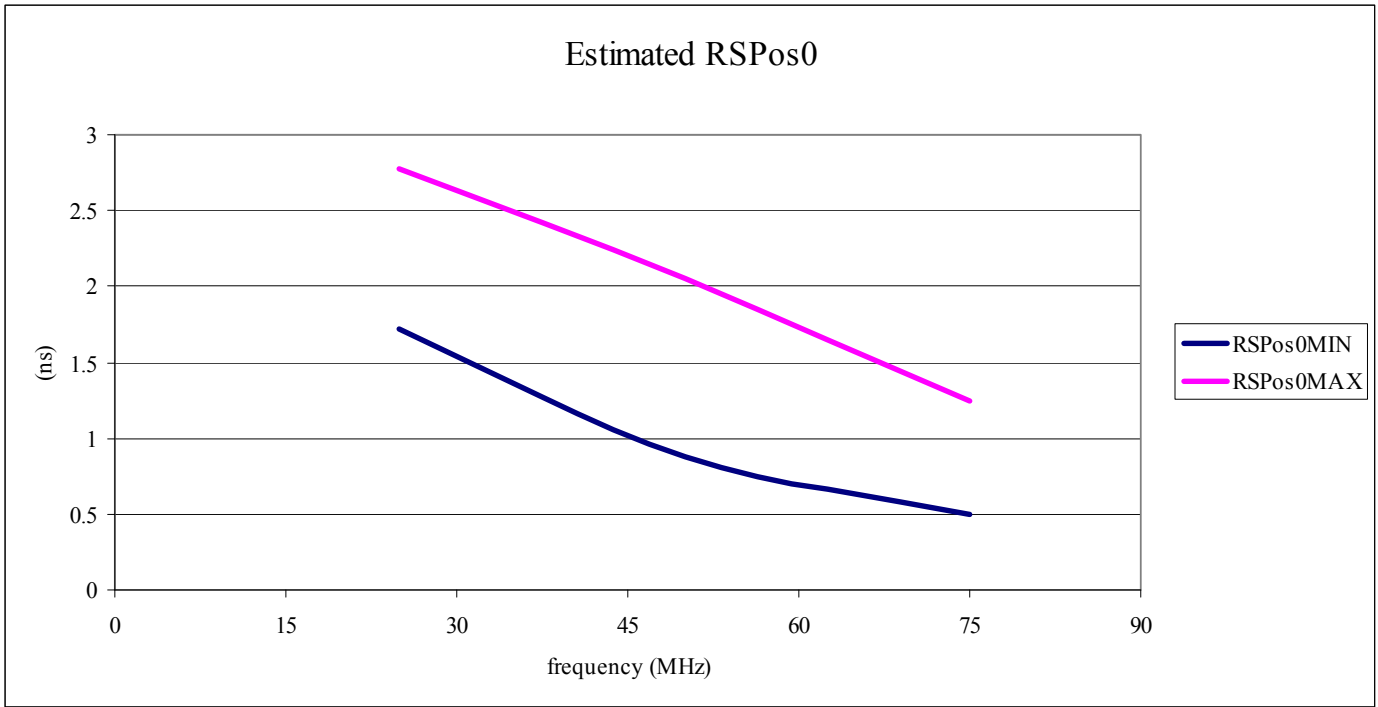


Figure 11. Estimated RSPos0 over frequency

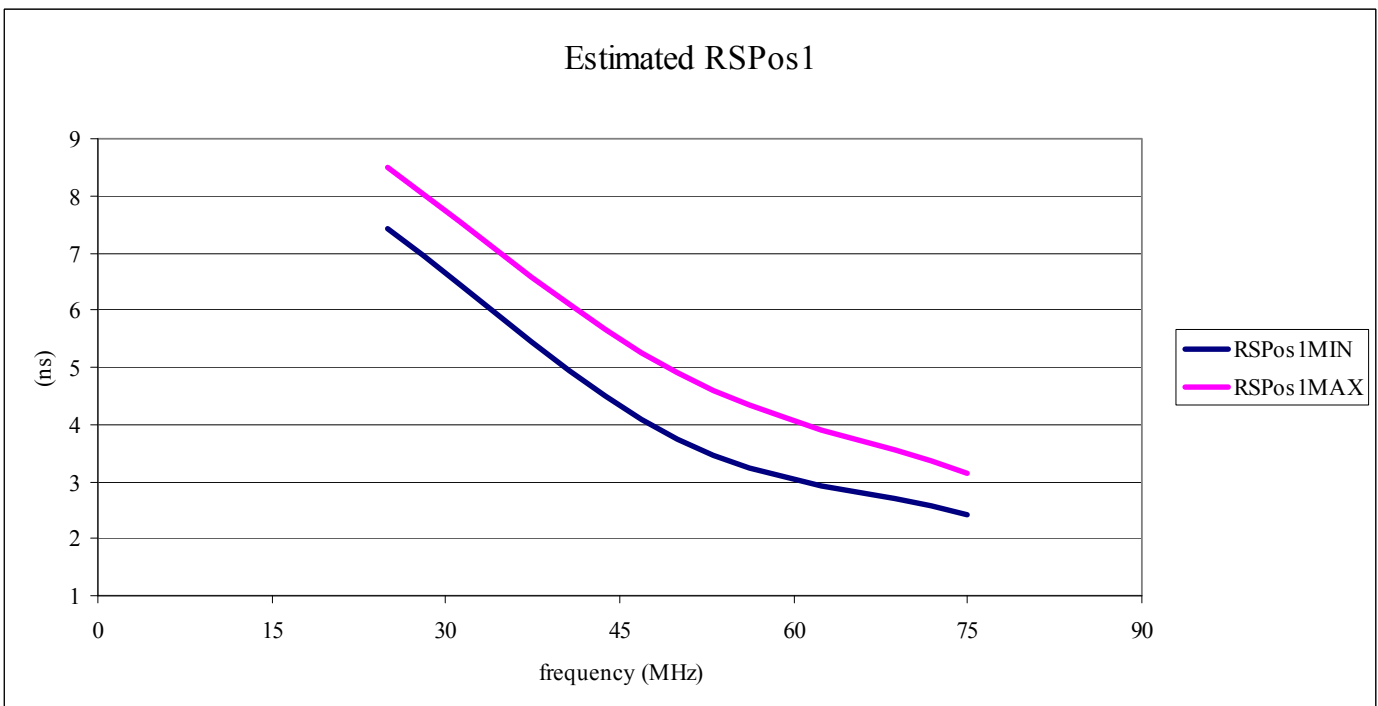


Figure 12. Estimated RSPos1 over frequency

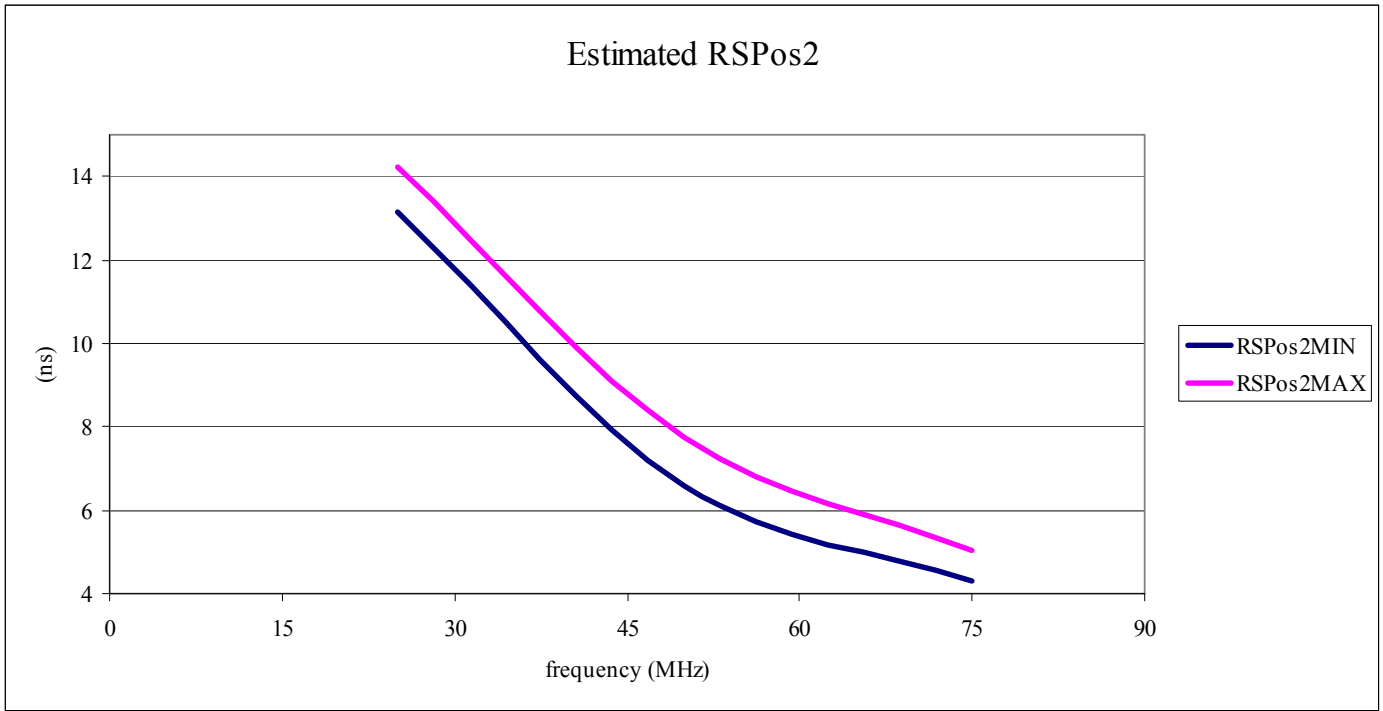


Figure 13. Estimated RSPos2 over frequency

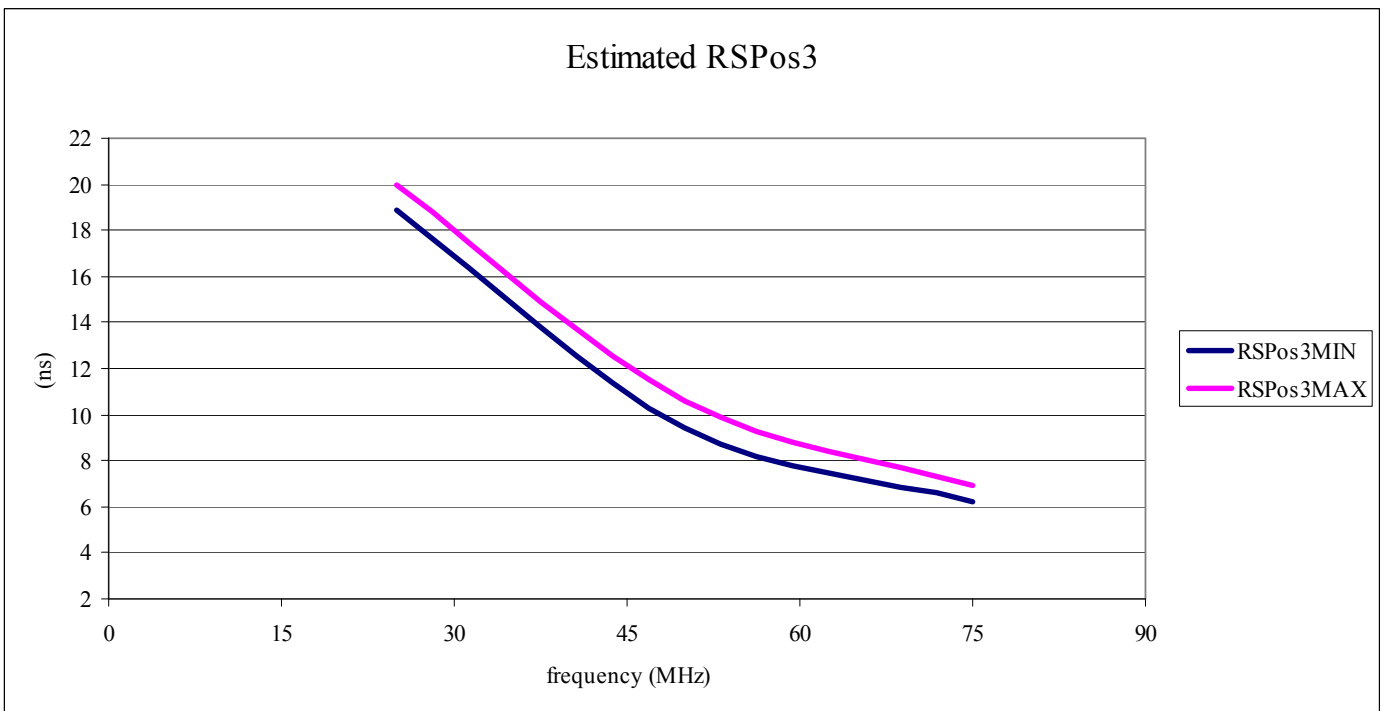


Figure 14. Estimated RSPos3 over frequency

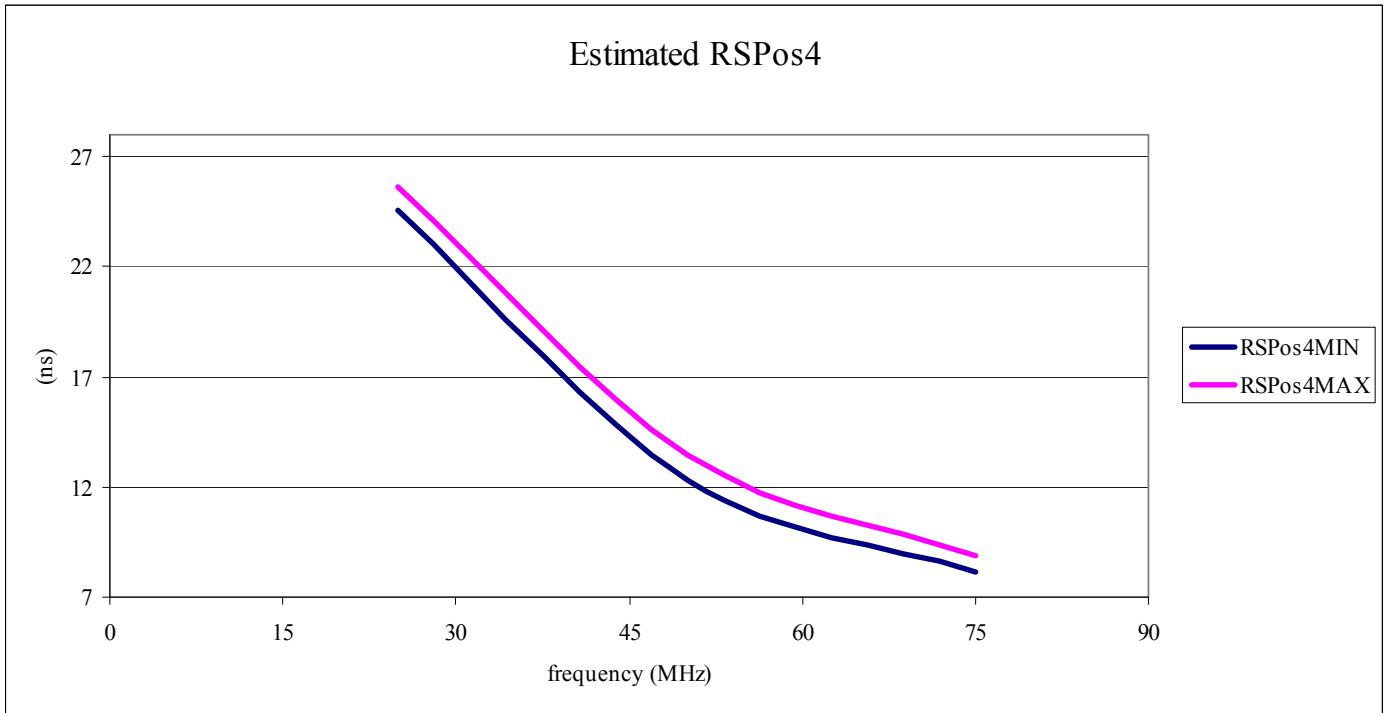


Figure 15. Estimated RSPos4 over frequency

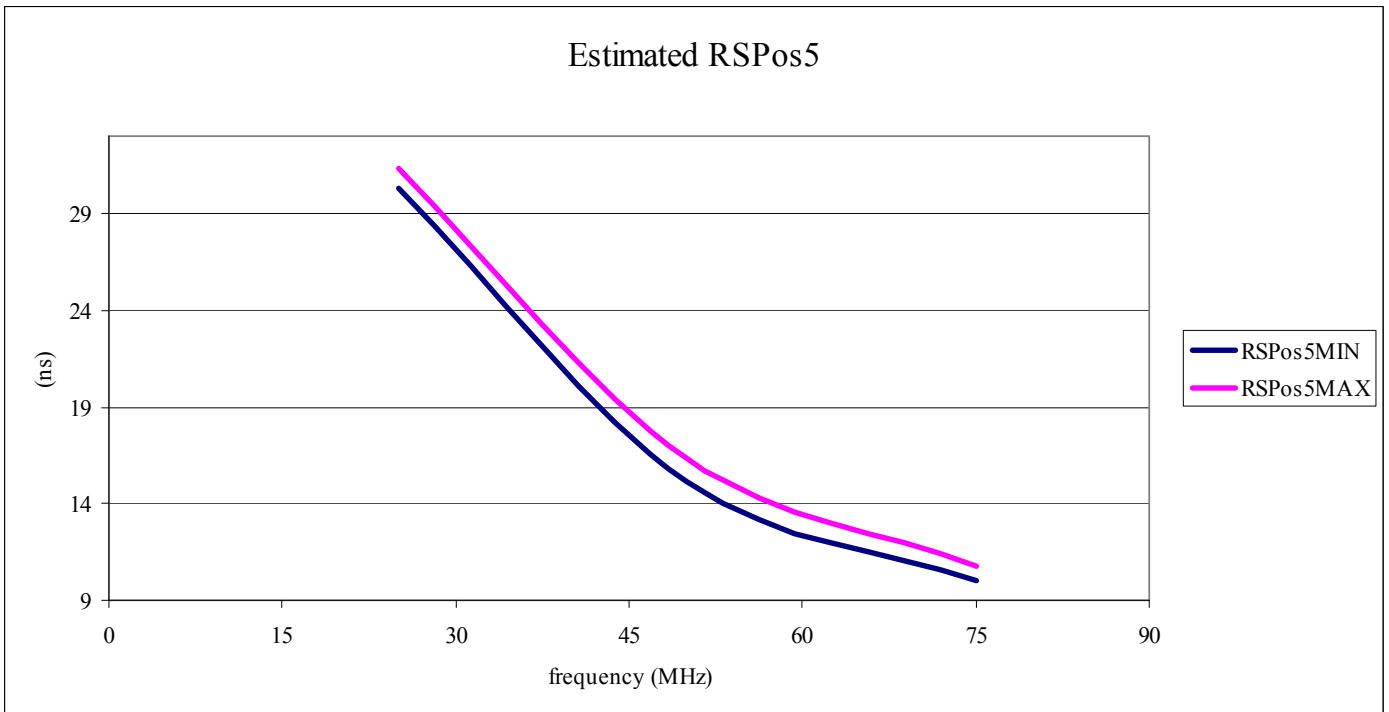


Figure 16. Estimated RSPos5 over frequency

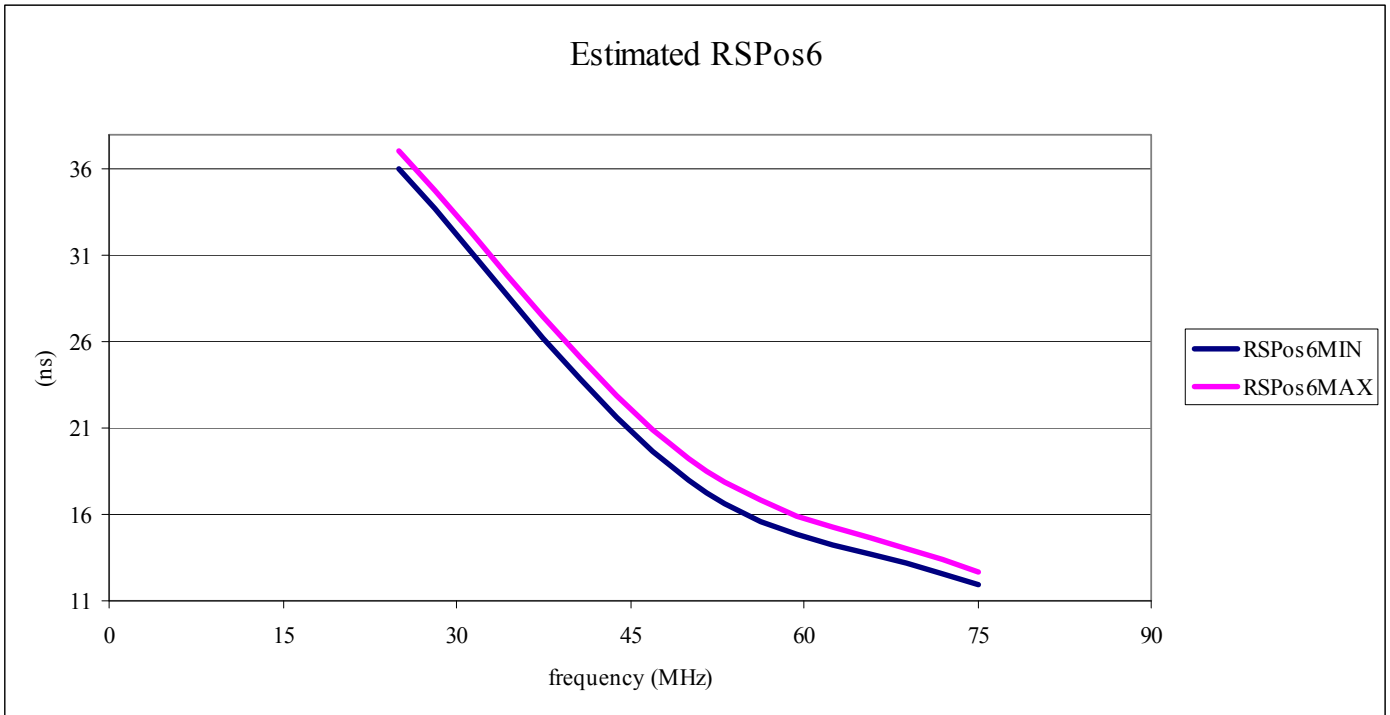


Figure 17. Estimated RSPos6 over frequency

### 3.0 Summary

Having estimates for TPosN and RSPosN for various clock frequencies aids the system designer in figuring system timing requirements and calculating RSKM at frequencies in the range of 25 to 75MHz.

See APP-LVDS-012 for an example of how to calculate RSKM.