

Recommended Serializer/Deserializer Power on Sequence

Table 1: Cross Reference of Applicable Products

Product Name:	Manufacturer Part Number	SMD #	Device Type	Internal PIC*
Serializer 3.3-Volt with Cold Spare all pins	UT54LVDS217	5962-01534	01, 02	WD11, WD13
Deserializer 3.3-Volt with Cold Spare all pins	UT54LVDS218	5962-01535	01, 02	WD12, WD14

*PIC = Product Identification Code

1.0 Overview

When applying power to the UT54LVDS218 Deserializer before the UT54LVDS217 Serializer, there is a possibility the UT54LVDS218 PLL could synchronize to periodic noise on the bus. When the serializer is powered, the UT54LVDS218 (218) will have to re-synchronize with the UT54LVDS217 (217) clock. To ensure proper functionality, Aeroflex Colorado Springs recommends the following power on sequence for the 217 and 218.

2.0 Recommended Power up Sequence

Assuming V_{DD} and PLL V_{DD} are tied together; apply power to both the 217 and 218 at the same time. Ensure the /PWRDWN pins for both devices are equal to V_{SS} . If powering the 217 and 218 at the same time is not feasible, power the 217 to nominal V_{DD} before powering the 218. Clock and data inputs (TxCLK IN and TxIN[20:0]) may be applied prior to, simultaneously, or after the 217 is powered up. Once V_{DD} and PLL V_{DD} for the 217 stabilize, the /PWRDWN pin should be switched from V_{SS} to V_{DD} . After ~10ms (TPLLS) the PLL will be locked and valid clock and data is present on the TxCLK+/- and TxOUT+/-[2:0] of the serializer. After the 217 Serializer is stable apply V_{DD} and PLL V_{DD} to the 218, once the supply for the Deserializer is stable, the /PWRDWN pin should be switched from low to high (V_{SS} to V_{DD}). After ~10ms (RPLLS) the PLL of the 218 will be locked and valid clock and data is present on the RxCLK OUT and RxOUT[20:0] of the Deserializer. Following this sequence ensures the PLL will properly achieve lock. See Figure 1.

1. Ensure /PWRDWN on 217 and 218 are equal to V_{SS}
- ** TxCLK IN and TxIN[20:0] may be applied prior to, simultaneously, or after the 217 is powered up
2. Apply power to UT54LVDS217 ($V_{DD} = \text{PLL } V_{DD}$)
3. Allow 217 to stabilize
4. Set /PWRDWN on 217 to V_{DD}
5. After TPLLS (~10ms) valid clock and data will be present on TxCLK+/- and TxOUT+/-[2:0]
6. Power on UT54LVDS218 ($V_{DD} = \text{PLL } V_{DD}$)
7. Allow 218 to stabilize
8. Set /PWRDWN on 218 to V_{DD}
9. After RPLLS (~10ms) valid data will be present on the RxCLK OUT and RxOUT[20:0] pins

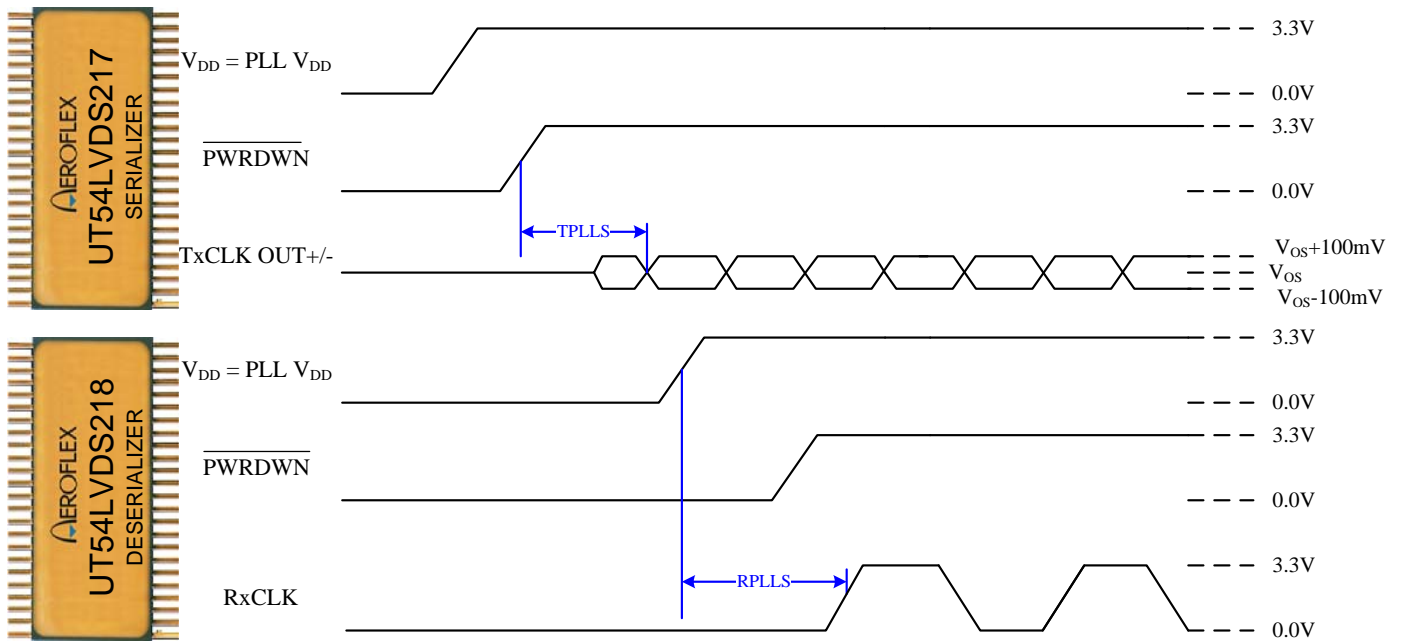


Figure 1. Notional Recommended Power up Sequence