

UT1553B BCRT TO 80186 INTERFACE

INTRODUCTION

The UTMC UT1553B BCRT is a monolithic CMOS integrated circuit that provides comprehensive Bus Controller and Remote Terminal functions for MIL-STD-1553B. The BCRT design reduces the overhead placed on the host computer by automatically executing message transfers, providing interrupts, and generating status information. The BCRT offloads the host processor with built-in memory management functions designed specifically for MIL-STD-1553B applications. Thus the host need only establish the necessary data and/or control parameters in memory so that the BCRT can access the information as required and therefore provide the requisite bus functions.

This application note outlines a simple pseudo-dual-port RAM memory interface for the BCRT to be used in conjunction with a 80186 microprocessor. A DMA interface will also be discussed.

The information supplied in this note is entirely applicable to other members of the UTMC BCRT family. This family includes the BCRTM (a BCRT with Monitor functions) and the BCRTMP (a BCRT which operates with a wide variety of avionics serial bus protocols).

DESIGN SELECTIONS

The 80186 processor provides the designer with a number of convenient signals for selecting memory and I/O ports. In this application note, the BCRT's registers are in peripheral space. 8K x 16 of static RAM is in the 80186's software programmable "mid-range" memory space. 8K of memory is sufficient for most 1553 applications, but any amount of memory can be used without affecting this design.

PSEUDO-DUAL-PORT RAM ARCHITECTURE

The BCRT is equipped with signals for implementing a pseudo-dual-port design with ease. The input signals are \overline{RD} , \overline{WR} , and $\overline{MEMCS1}$. The output signals are \overline{RRD} , \overline{RWR} , and $\overline{MEMCS0}$. When the BCRT is not accessing memory, indicated by \overline{DMACK} high, the inputs are passed through to the outputs. When \overline{DMACK} is low, the inputs are blocked. To generate wait states, an arbitration device controls the 80186's \overline{SRDY} signal. The same device controls access to the BCRT by the 80186, and to the memory by the BCRT. Figure 1 shows the input and output signals to this device.

ARBITRATION DETAILS

The arbitration algorithm can be accomplished in a small programmable logic device such as a 22V10. Figure 2 shows a description of the state machine necessary through the use of a state diagram and state table. The state machine is designed to change states on the rising edges of \overline{CLKOUT} .

A request by the 80186 is defined as the assertion of either $\overline{MCS0}$ in the case of a memory access or $\overline{PCS0}$ in the case of a BCRT access. Since either access requires use of the shared address and data buses, they are treated identically. A request by the BCRT is defined as the assertion of its \overline{DMAR} signal.

Upon reset, the arbitration state machine (ASM) goes to state *a*. It remains in this state until one of three possible conditions:

1. the BCRT requests
2. the 80186 requests
3. both 1 & 2

In case 1, the ASM goes to state *c*. Here, \overline{DMAG} is asserted. Upon receiving \overline{DMAG} , the BCRT asserts \overline{DMACK} . The ASM remains in state *c* until one of three events occur:

- 1.1. the BCRT deasserts \overline{DMACK}
- 1.2. the 80186 requests
- 1.3. both 1 & 2

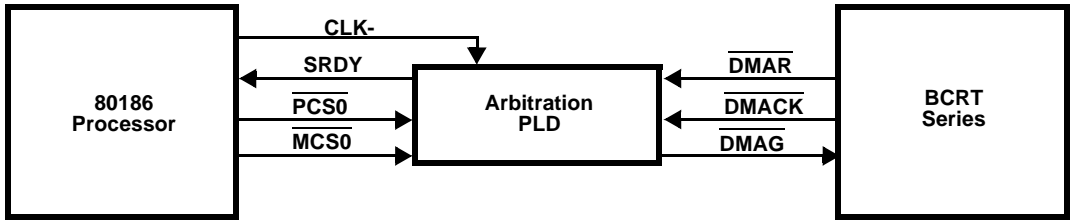
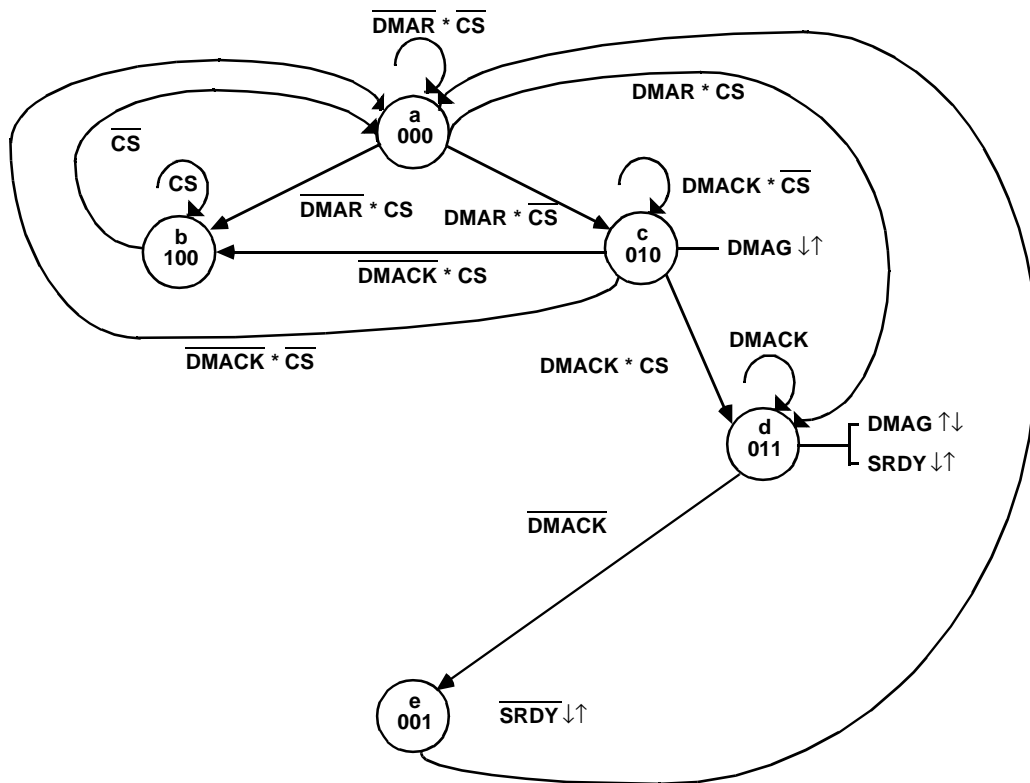


Figure 1. Arbitration PLD Inputs and Outputs



Notes:

1. $CS = MCS0 + PCS0$.
2. All signals in this diagram have been converted to positive logic; thus DMAR indicates the asserted (low) state and \overline{DMAR} indicates the deasserted (high) state of the actual signal.
3. SRDY must be synchronized to CLKOUT.

Figure 2. Arbitration PLD Description

	CURRENT STATE			INPUTS			NEXT STATE			OUTPUTS		
	S ₀	S ₁	S ₂	DMAR	CS	DMACK	S ₀	S ₁	S ₂	DMAG	SRDY	
a	0	0	0	0	0	X	a	0	0	0	0	0
a	0	0	0	0	1	X	b	1	0	0	0	0
a	0	0	0	1	0	X	c	0	1	0	0	0
a	0	0	0	1	1	X	d	0	1	1	0	0
b	1	0	0	X	1	X	b	1	0	0	0	0
b	1	0	0	X	0	X	a	0	0	0	0	0
c	0	1	0	X	0	0	a	0	0	0	1	0
c	0	1	0	X	1	0	b	1	0	0	1	0
c	0	1	0	X	0	1	c	0	1	0	1	0
c	0	1	0	X	1	1	d	0	1	1	1	0
d	0	1	1	X	X	0	e	0	0	1	1	1
d	0	1	1	X	X	1	e	0	1	1	1	1
e	0	0	1	X	X	X	a	0	0	0	0	1

In case 1.1, the BCRT returns to idle state *a*. In case 1.2, the ASM advances to state *d*, where SRDY is deasserted causing the 80186 to wait until the BCRT is finished. The ASM stays in state *d* until DMACK is deasserted, at which time it advances to state *e*. In this state, the address buffers switch back to 80186 control. The data the processor is trying to read or write is passed. The ASM then returns to state *a*, where the SRDY is asserted and the 80186 completes its cycle.

In case 1.3, the 80186 requests access in the same cycle that the BCRT has completed. In this case, state *b* is entered and the processor performs a cycle as if the ASM had started from an idle state.

In case 2 from above, the 80186 requests from an ASM idle state. In this case, the ASM goes to state *b*. State *b* prevents the BCRT from receiving a DMAG. On the next cycle, the 80186 cycle is complete and the ASM returns to idle state. For slower memories, wait states may be added (with SRDY deasserted) between *a* and *b*. However, care must be taken not to exceed the maximum DMAR to DMAG times given in the BCRT data sheet.

In case 3 from above, the BCRT and 80186 request at the same time. In this case, the BCRT wins and the 80186 must wait (entering state *d*).

Figures 4 and 5 show timing diagrams for each of the possible arbitration scenarios. These diagrams show the transitions on a cycle-by-cycle basis of CLKOUT. For exact timing delays for the 80186 or BCRT, consult the appropriate data sheet.

MEMORY CONTROL/ACCESS LOGIC

Figure 3 shows the connection of the remaining control signals required in this interface. Note the use of bus transceivers and latches to demultiplex the 80186 address/data bus. Also note the use of the RD, WR, MEMCSI, RRD, RWR, and MEMCSO signals. If additional memory devices or other peripherals are to be placed in the 80186 system, they should have separate bus transceivers and latches.

DMA CONFIGURATION

If additional memory devices and other peripherals are put on the shared address/data bus shown in the diagram, the pseudo-dual-port design is essentially converted to DMA configuration. The arbitration algorithm must now be used for all 80186 accesses. In this configuration, the BCRT lacks a "local" data bus, eliminating several bus buffers and latches. The disadvantage to this approach is that the BCRT data transfers now compete with non-1553-related activity on the host bus. In systems with low bus throughput, this alternative may be an acceptable.

SUMMARY

This note has shown a simple pseudo-dual-port RAM implementation for a BCRT to 80186 interface. A separate application note is available discussing a true dual-port configuration.

For further information on UTMC products and literature, please contact UTMC applications support.

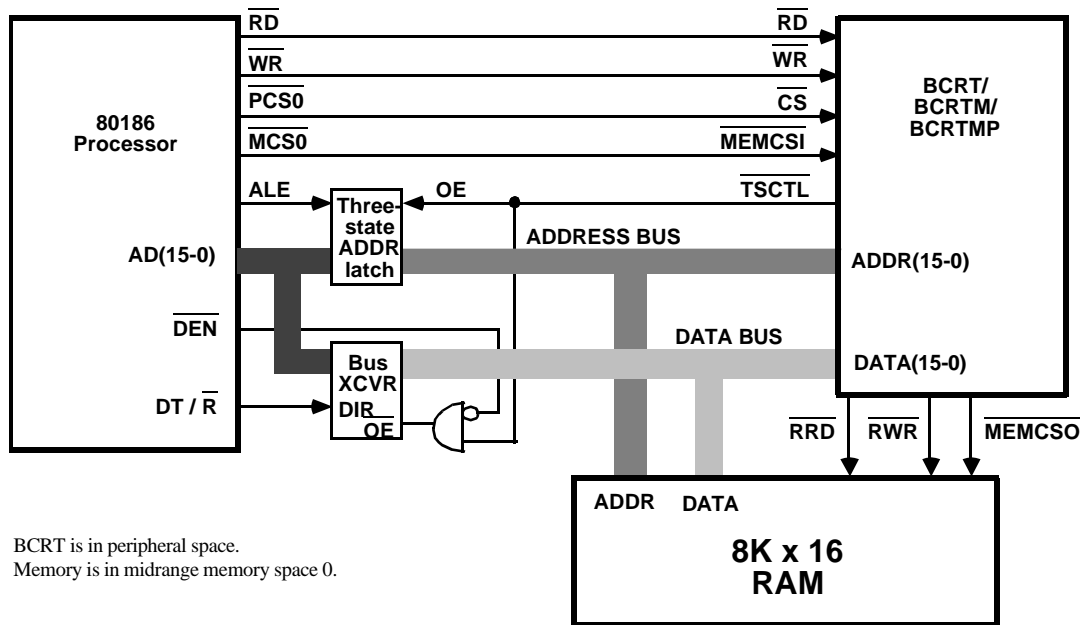
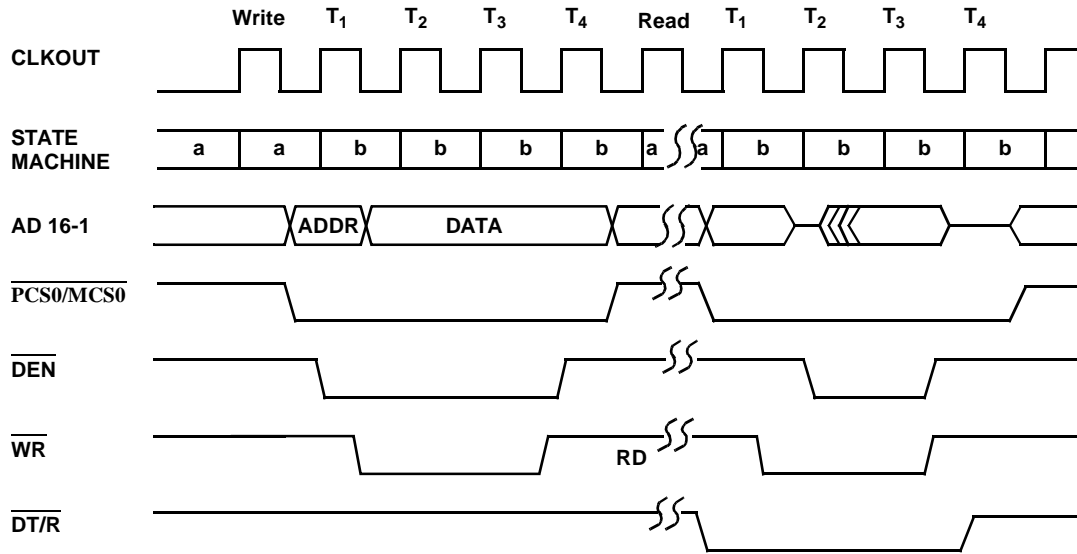


Figure 3. System-Level Control Signals

80186 Access with no Arbitration



Note:
 If the BCRTM asserts \overline{DMAR} while the state machine is in state b, it will have to wait until the state machine returns to state a before its request will be processed. (Processing then continues as shown below.)

BCRTM Access with no Arbitration

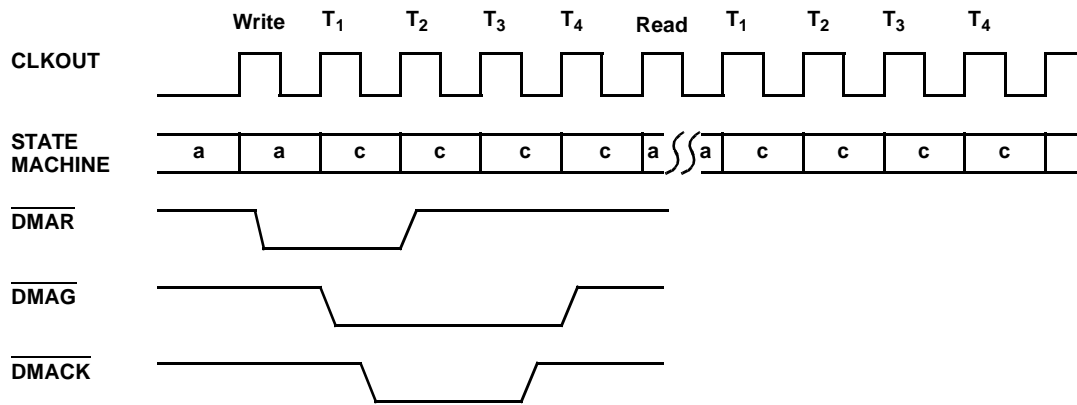
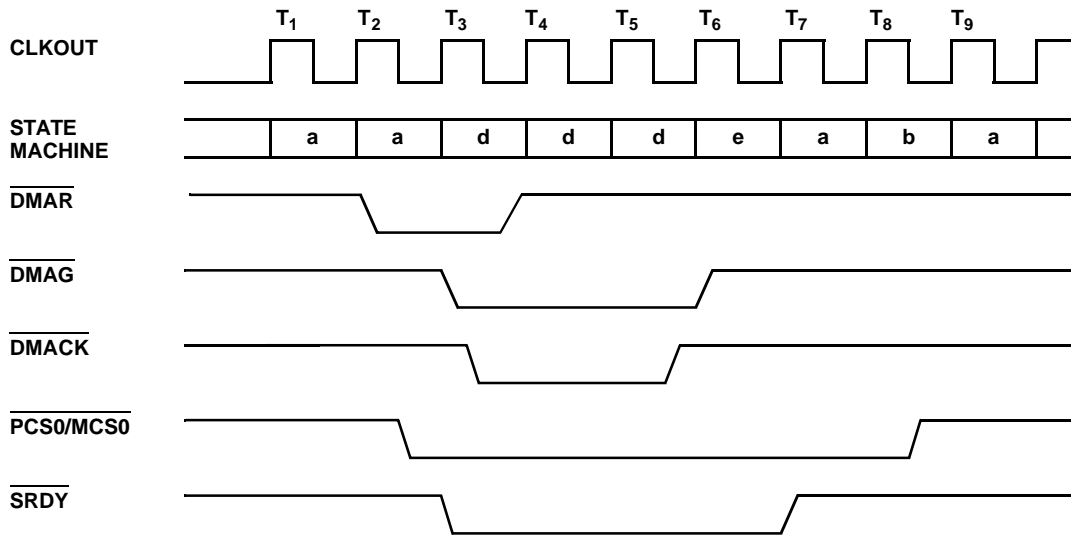


Figure 4. Arbitration Timing Diagram

80186/BCRTM Request at Same Time



80186 Requests While BCRTM is using the Bus (BCRTM is on Last Cycle)

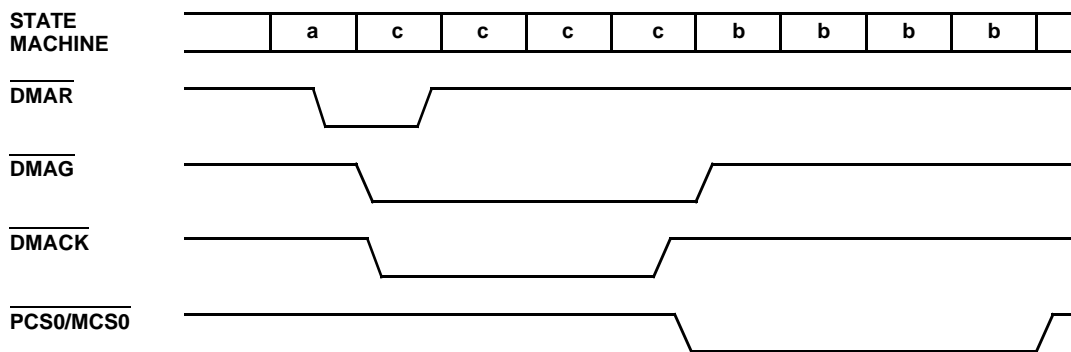


Figure 5. Arbitration Timing Diagram

80186 Requests While BCRT is using the Bus (BCRTM is not on Last Cycle)

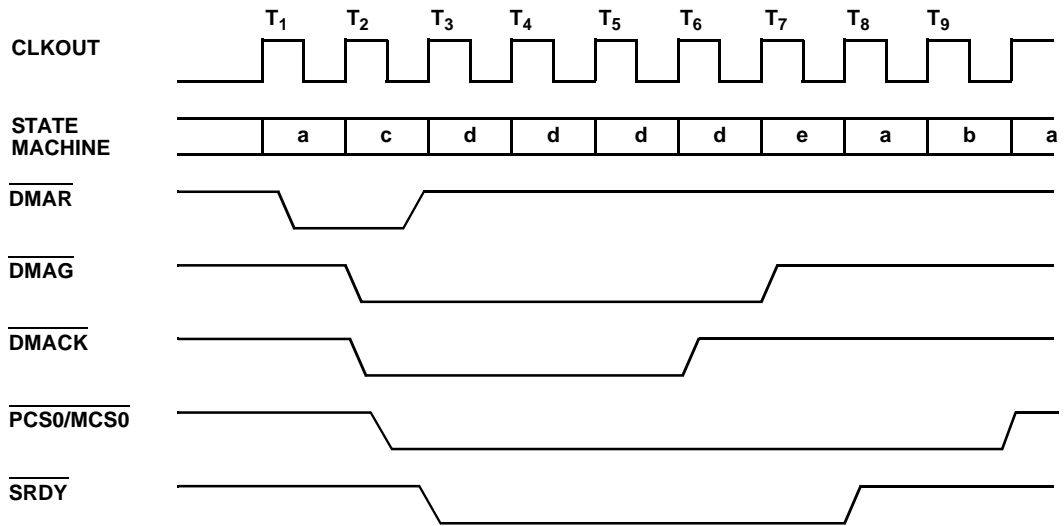


Figure 5. Arbitration Timing Diagram (cont.)