

UTMC APPLICATION NOTE

Interfacing the BCRT to the 68000 16-Bit MPU

INTRODUCTION

The UTMC UT1553B BCRT is a monolithic CMOS integrated circuit that provides comprehensive MIL-STD-1553B Bus Controller and Remote Terminal functions. The BCRT design reduces the host computer's overhead requirements by automatically executing message transfers, providing interrupts, and generating status information. The BCRT accomplishes much of this off-loading with built-in memory management functions designed specifically for MIL-STD-1553B applications. This means the host need only establish the necessary data and/or control parameters in memory for the BCRT to access the information as required, thus providing the requisite MIL-STD-1553B bus functions.

Back to Basics

Several terms and concepts are involved in describing a multimaster microprocessor-based system. A bus master is a device capable of controlling the Address, Data, and Control buses. A multimaster system contains two or more master devices. Only one bus master can control the bus at any given time.

DMA Configuration

The BCRT interfaces easily into a 68000-based system. Except for the 68000 processor, the DMA configuration assigns the BCRT as the highest priority bus master in a multimaster system. This configuration requires using one or more 68000 processors, one or more BCRTs, and could

also contain other bus masters. The following sections define the architecture of a system containing only two bus masters: a BCRT and a 68000.

DMA Arbitration

The process of the BCRT assuming control of the bus while another master relinquishes control is called DMA arbitration. Figure 1 depicts a DMA arbitration sequence. Three signals are involved in the arbitration process: $\overline{\text{DMAR}}$ (DMA Request), $\overline{\text{DMAG}}$ (DMA Grant), and $\overline{\text{DMACK}}$ (DMA Acknowledge). The requesting device asserts $\overline{\text{DMAR}}$ when it needs to control the bus. The controlling device recognizes the $\overline{\text{DMAR}}$ assertion and generates $\overline{\text{DMAG}}$ when it is finished with the bus. The requesting device deasserts $\overline{\text{DMAR}}$ and asserts $\overline{\text{DMACK}}$. The arbitration is now complete and the requesting device has become the controlling bus master.

The other signals associated with DMA are $\overline{\text{DMAGO}}$, BURST, and $\overline{\text{TSCTL}}$. The $\overline{\text{DMAGO}}$ signal is for serially chaining multiple bus masters. The $\overline{\text{DMAGO}}$ signal passes the $\overline{\text{DMAG}}$ signal if the BCRT is not requesting the bus when $\overline{\text{DMAG}}$ is asserted. The BURST signal is an active high signal that indicates the current DMA cycle will transfer at least two words (worst case is five words). The $\overline{\text{TSCTL}}$ (Three-State Control) signal indicates when the BCRT is actually accessing memory. The host system's address and data lines must be in the high-impedance state when this signal is active.

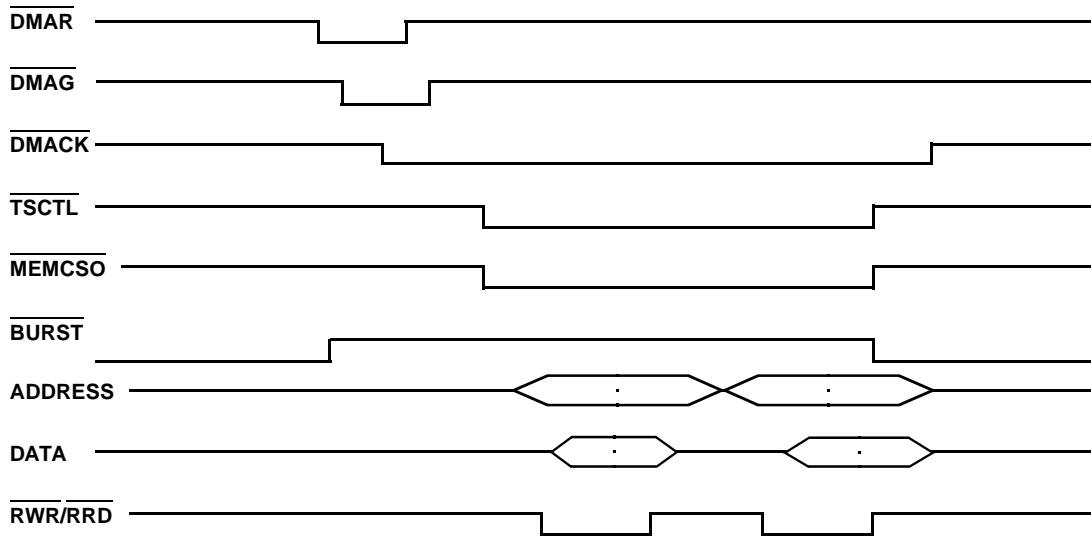


Figure 1. DMA Timing (Refer to BCRT Data Sheet for Detailed Timing Information)

BCRT Memory Bus Signals

The BCRT bus signals are split into three groups: Address, Data, and Control. Four bidirectional signals (A0-A3) and 12 three-state signals (A4-A15) comprise the Address bus. The word size for the BCRT is always sixteen bits. The 68000 processor address references must be divided by two when compared to the BCRT. The Data bus consists of 16 bidirectional signals numbered D0 through D15. The memory control signals consist of \overline{RRD} (RAM Read) and \overline{RWR} (RAM Write). \overline{RRD} pulses low during a DMA read operation, and \overline{RWR} pulses low during a write operation. Figure 1 represents DMA read and write operations. Consult the UT1553B BCRT data sheet for actual timing relationships.

DMA Hardware Configuration

Figure 2 illustrates the DMA interface signal connections for a two-master system containing a 68000 and a BCRT. Four signals are involved: \overline{DMAR} is connected to \overline{BR} (Bus Request), \overline{DMAG} is connected to \overline{BG} (Bus Grant), \overline{DMACK} is connected to \overline{BGACK} (Bus Grant Acknowledge), and \overline{AEN} is tied high.

Figure 3 is a block diagram illustrating the DMA and memory signals. Figure 4 shows a simplified circuit diagram containing the BCRT and 68000, along with a bank of static memory devices.

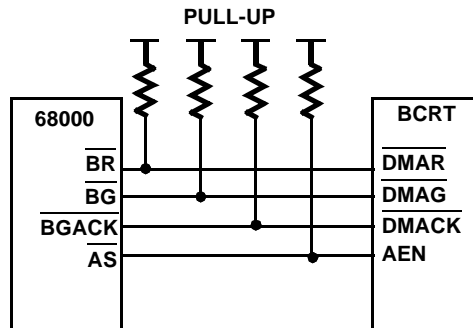


Figure 2. DMA Interface Signal Connections

CONCLUSION

This application note presents a system configuration example of the UT1553B BCRT'S interface to a typical 16-bit microprocessor using the 68000 as the processor. This information also applies to a wide variety of other microprocessors. For more detailed information on the UT1553B BCRT or other UTMC products.

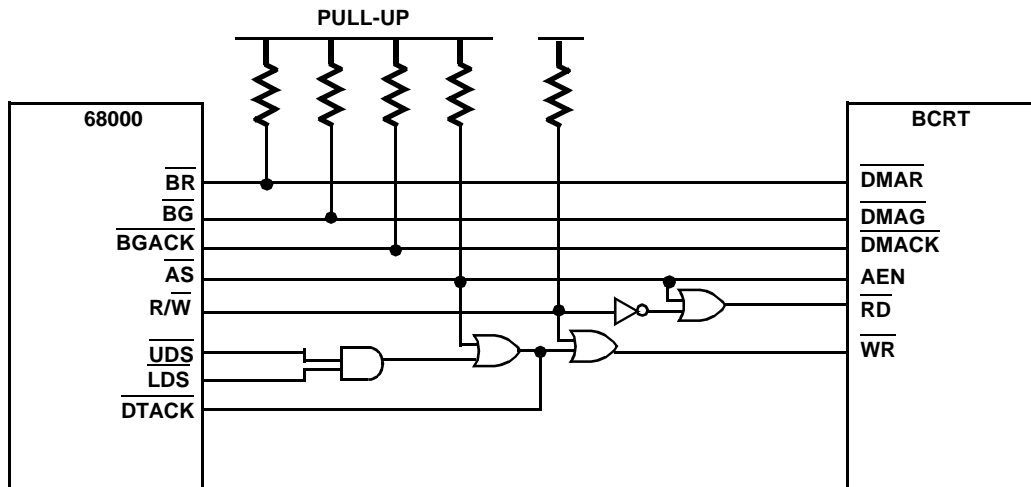


Figure 3. DMA and Memory Interface Signal Connections

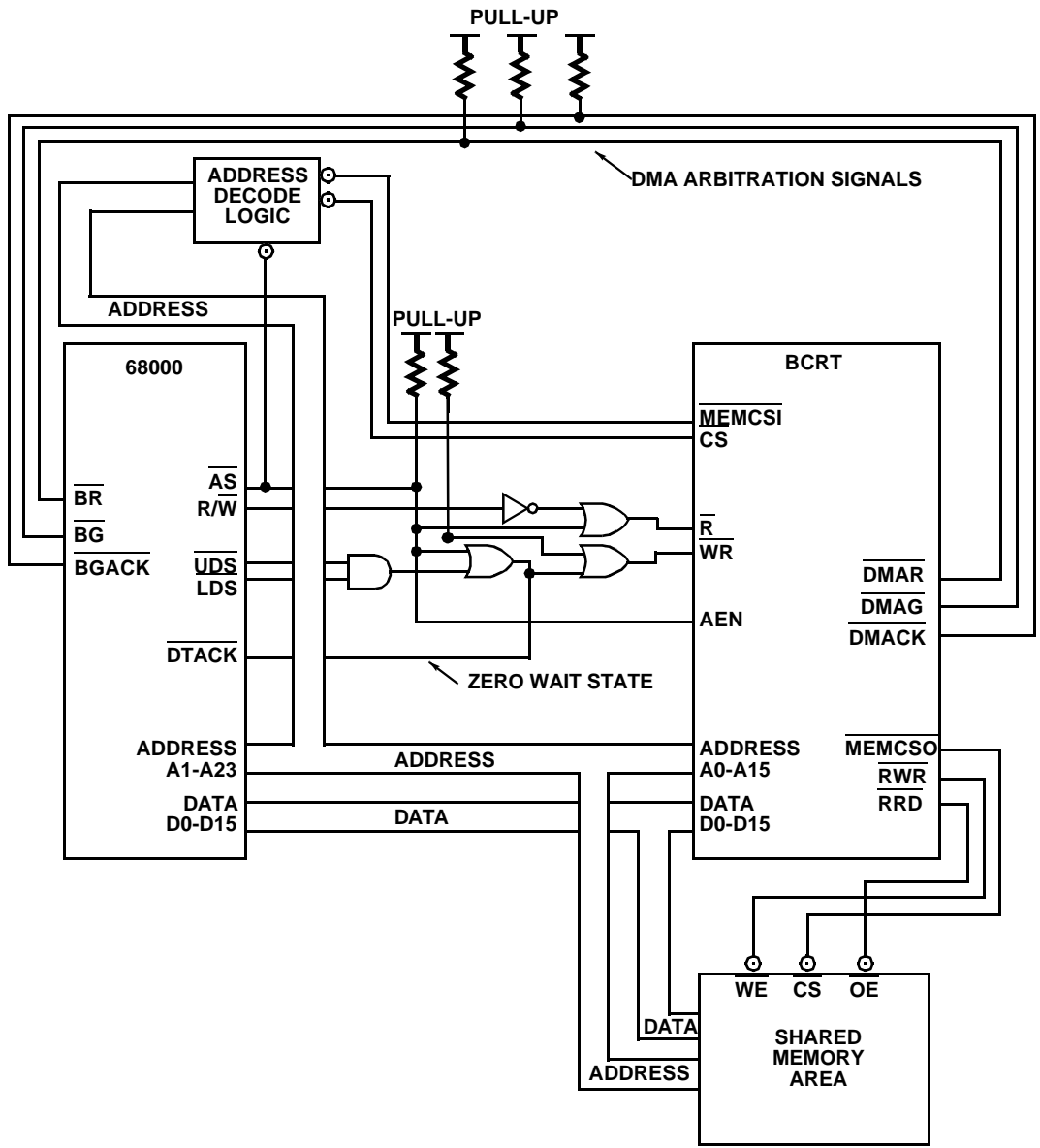


Figure 4. DMA Configuration