March 15, 2010

Radiation Performance Data Package

MUX8533-S

MUX8533-S DSCC SMD Part Number: 5962-0923202KXC

Dual 16 channel analog multiplexer,
high impedance analog input with ESD protection.

Prepared by:

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1. MUX8533-S:

1.1 Part Description

1.1.1 Dual 16 channel analog multiplexer, high impedance analog input with ESD protection.

1.2 Applicable Documents

1.2.1	Appendix A:	Data Sheet:	MUX8533	Dual 16-Channel Analog Multiplexer Module, Radiation Tolerant & ESD Protected
1.2.2	Appendix B:	NESREC:	NGCP3580	A Radiation Hardened High Voltage 16:1 Analog Multiplexer for Space Applications
1.2.3	Appendix C:	DSCC SMD:	5962-09232	MICROCIRCUIT, HYBRID, LINEAR, DUAL 16 CHANNEL, ANALOG MULTIPLEXER

2. Radiation Performance

2.1 Total Dose: 150 krads(Si), Dose rate = 50 - 300 rads(Si)/s

2.1.1 Every wafer lot is subjected to RLAT testing at the stated total dose and dose rate.

2.2 SEU: Immune: Tested to 90 MeV-cm^2/mg

2.2.1 See Appendix B: 2008 NSREC Radiation Effects Data Workshop Proceedings, pp 82-84.

2.3 SEL: Immune, guaranteed by process design

2.3.1 See Appendix B: 2008 NSREC Radiation Effects Data Workshop Proceedings, pp 82-84.

Standard Products

MUX8533 Dual 16-Channel Analog Multiplexer Module Radiation Tolerant & ESD Protected

www.aeroflex.com/mux

April 20, 2009

FEATURES

- 32-channels provided by two independent 16-channel multiplexers
- Radiation performance
  - Total dose: 150 krads(Si), Dose rate = 50 - 300 rads(Si)/s
  - SEU: Immune up to 90 MeV-cm^2/mg
  - SEL: Immune by process design
- Full military temperature range
- Low power consumption < 30mW
- Separate address bus and enable line for CH0-15 and CH16-31
- Fast access time < 500ns typical
- All channel inputs protected by ±20V nominal Transorbs
- Input over voltage protection (power on or off)
- Break-Before-Make switching
- High analog input impedance (power on or off)
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic ceramic
  - 56 leads, 0.80"Sq x 0.20"Ht quad flat pack
  - Typical Weight 6 grams
- DSCC SMD 5962-09232 pending

Note: Aeroflex Plainview does not currently have a DSCC certified Radiation Hardened Assurance Program.

GENERAL DESCRIPTION

Aeroflex's MUX8533 is a radiation tolerant, Dual 16 channel multiplexer MCM (Multi Chip Module) with electrostatic discharge (ESD) protection on all channel inputs.

The MUX8533 has been specifically designed to meet exposure to radiation environments. It is available in a 56 lead High Temperature Co-Fired Ceramic (HTCC) Quad Flatpack (CQFP). It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534, the MUX8533 is ideal for demanding military and space applications.

ORGANIZATION AND APPLICATION

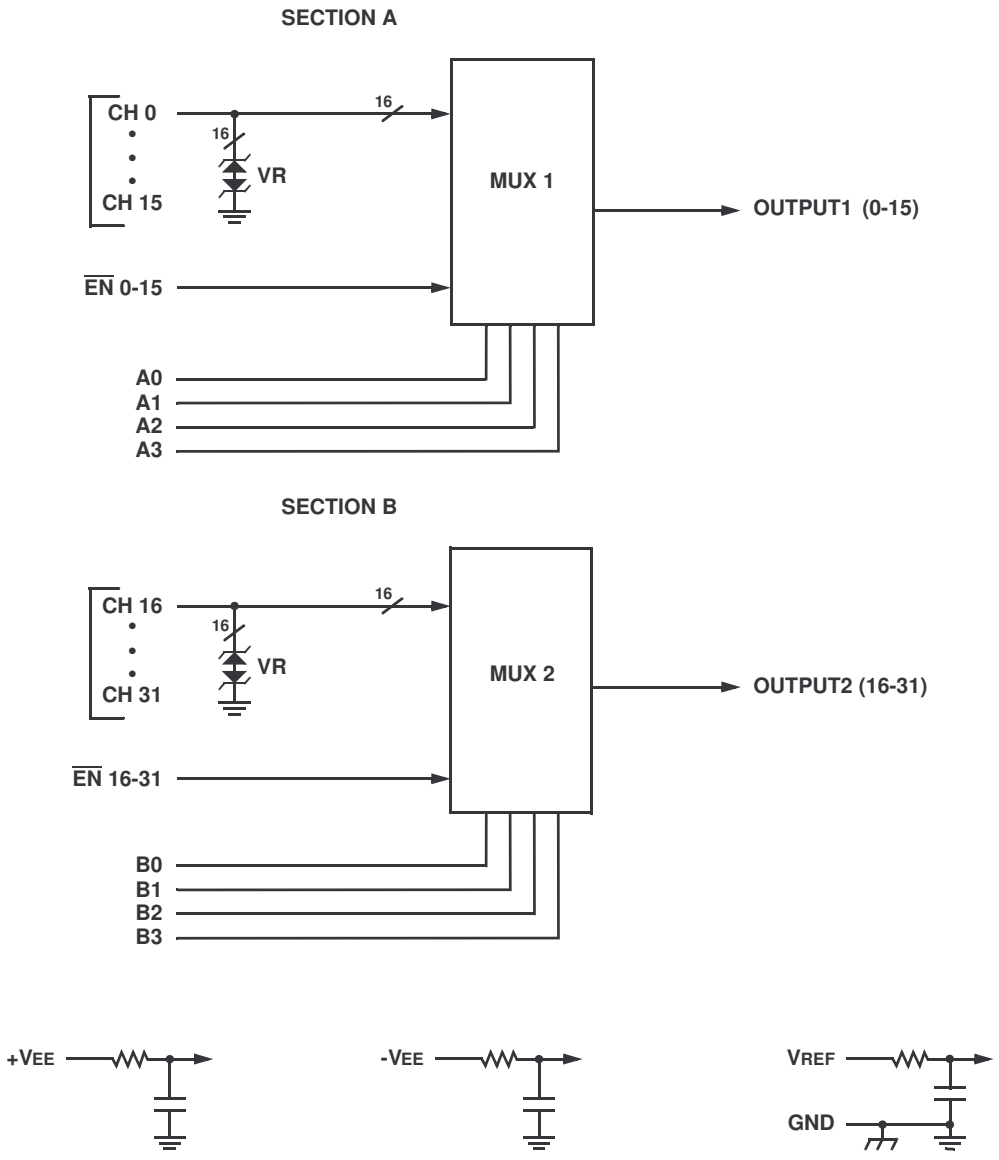
The MUX8533 consists of two separate and independent 16 channel multiplexers arranged as shown in the block diagram.

A Section

Sixteen (16) channels addressable by bus A_0~A_3, enabled by $\overline{EN}$0-15 and outputted on Output 1 (0-15).

B Section

Sixteen (16) channels addressable by bus B_0~B_3, enabled by $\overline{EN}$16-31 and outputted on Output 2 (16-31).



MUX8533: DUAL 16 CHANNEL ANALOG MUX BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS 1/

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	℃
Storage Temperature Range	-65 to +150	℃
Supply Voltage +VEE (Pin 18) -VEE (Pin 46) VREF (Pin 39)	 +20 -20 +7.5	 V V V
Digital Input Overvoltage VEN0-15 (Pin 13), VEN16-31 (Pin 44), VA (Pins 14, 15, 16, 17), VB (Pins 40, 41, 42, 43)	< VREF +.5 > GND -.5	V V
Analog Input Over Voltage VS	±18V	V

Notes:
1/ All measurements are made with respect to ground.

NOTICE: Stresses above those listed under "Absolute Maximums Rating" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

RECOMMENDED OPERATING CONDITIONS 1/

Symbol	Parameter	Typical	Units
+VEE	+15V Power Supply Voltage	+15.0	V
-VEE	-15V Power Supply Voltage	-15.0	V
VREF	Reference Voltage	+5.00	V
VAL	Logic Low Level	+0.8	V
VAH	Logic High Level	+4.0	V

1/ Power Supply turn-on sequence shall be as follows: -VEE, VREF, followed by +VEE.

DC ELECTRICAL PERFORMANCE CHARACTERISTICS 1/

(TC = -55℃ TO +125℃, -VEE = -15V, VREF = +5.0V, +VEE = +15V - UNLESS OTHERWISE SPECIFIED)

Parameter	Symbol	Conditions	Min	Max	Units
Supply Current	+IEE	VEN(0-15) = VEN(16-31) = VA(0-3) = VB(0-3) = 0	0	1	mA
	-IEE	VEN(0-15) = VEN(16-31) = VA(0-3) = VB(0-3) = 0	-1	0	mA
	+ISBY	VEN(0-15) = VEN(16-31) = 4V, VA(0-3) = VB(0-3) = 0 7/	0	1	mA
	-ISBY	VEN(0-15) = VEN(16-31) = 4V, VA(0-3) = VB(0-3) = 0 7/	-1	0	mA
Address Input Current	IAL(0-3)A	VA = 0V	-1	1	µA
	IAH(0-3)A	VA = 5V	-1	1	µA
	IAL(0-3)B	VB = 0V	-1	1	µA
	IAH(0-3)B	VB = 5V	-1	1	µA
Enable Input Current	IENL(0-15)	VEN(0-15) = 0V	-1	1	µA
	IENH(0-15)	VEN(0-15) = 5V	-1	1	µA
	IENL(16-31)	VEN(16-31) = 0V	-1	1	µA
	IENH(16-31)	VEN(16-31) = 5V	-1	1	µA

DC ELECTRICAL PERFORMANCE CHARACTERISTICS 1/ (continued)

(T_C = -55°C TO +125°C, $-V_{EE}$ = -15V, V_{REF} = +5.0V, $+V_{EE}$ = +15V - UNLESS OTHERWISE SPECIFIED)

Parameter	Symbol	Conditions		Min	Max	Units
Positive Input Leakage Current CH0-CH31	$+I_{SOFFOUTPUT(ALL)}$	V_{IN} = +10V, V_{EN} = 4V, output and all unused MUX inputs under test = -10V 2/, 3/		-100	+1000	nA
Negative Input Leakage Current CH0-CH31	$-I_{SOFFOUTPUT(ALL)}$	V_{IN} = -10V, V_{EN} = 4V, output and all unused MUX inputs under test = +10V 2/, 3/		-100	+1000	nA
Positive Output Leakage Current OUTPUTS (pins 12,45)	$+I_{DOFFOUTPUT(ALL)}$	V_{OUT} = +10V, V_{EN} = 4V, output and all unused MUX inputs under test = -10V 3/, 4/		-100	+100	nA
Negative Output Leakage Current OUTPUTS (pins 12,45)	$-I_{DOFFOUTPUT(ALL)}$	V_{OUT} = -10V, V_{EN} = 4V, output and all unused MUX inputs under test = +10V 3/, 4/		-100	+100	nA
Input Clamped Voltage CH0 - CH31	$+V_{CLMP}$	V_{EN} = 4V, all unused MUX inputs under test are open. 3/	+25°C +125°C -55°C	18.0 18.0 17.5	23.0 23.5 22.5	V V V
Input Clamped Voltage CH0 - CH31	$-V_{CLMP}$		+25°C +125°C -55°C	-23.0 -23.5 -22.5	-18.0 -18.0 -17.5	V V V
Switch ON Resistance OUTPUTS (pins 12,45) 6/	$R_{DS(ON)}(0\text{-}31)_A$	V_{IN} = +15V, V_{EN} = 0.8V, I_{OUT} = -1mA 2/, 3/, 5/		200	1000	Ω
	$R_{DS(ON)}(0\text{-}31)_B$	V_{IN} = +5V, V_{EN} = 0.8V, I_{OUT} = -1mA 2/, 3/, 5/		200	1500	Ω
	$R_{DS(ON)}(0\text{-}31)_C$	V_{IN} = -5V, V_{EN} = 0.8V, I_{OUT} = +1mA 2/, 3/, 5/		200	2500	Ω

Notes:

1/ Measure inputs sequentially. Ground all unused inputs of the device under test. V_A is the applied input voltage to the address lines A(0-3). V_B is the applied input voltage to the address lines B(0-3)

2/ V_{IN} is the applied input voltage to the input channels CH0-CH31.

3/ V_{EN} is the applied input voltage to the enable line EN (0-15) and EN (16-31).

4/ V_{OUT} is the applied input voltage to the output lines OUTPUT1 (0-15), OUTPUT2 (16-31)

5/ Negative current is the current flowing out of each of the MUX pins. Positive current is the current flowing into each MUX pin.

6/ The MUX8533 cannot be operated with analog inputs from -15 to -5 volts.

7/ Not tested, guaranteed to the specified limits.

SWITCHING CHARACTERISTICS

(T_C = -55°C TO +125°C, $-V_{EE}$ = -15V, V_{REF} = +5.0V, $+V_{EE}$ = +15V -- UNLESS OTHERWISE SPECIFIED)

Parameter	Symbol	Conditions	Min	Max	Units
Switching Test MUX	t_AHL	R_L = 10KΩ, C_L = 50pF	10	1000	ns
	t_ALH		10	1000	ns
	$t_{ON}EN$	R_L = 1KΩ, C_L = 50pF	10	1000	ns
	$t_{OFF}EN$		10	1000	ns

TRUTH TABLE (CH0 – CH15)

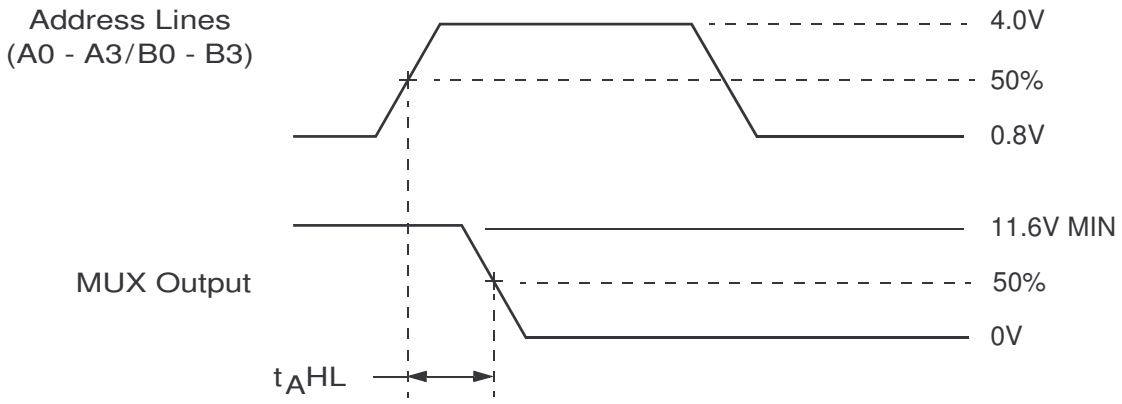
A3	A2	A1	A0	$\overline{EN}$ (0-15)	"ON" CHANNEL, 1/ (OUTPUT 1)
X	X	X	X	H	NONE
L	L	L	L	L	CH0
L	L	L	H	L	CH1
L	L	H	L	L	CH2
L	L	H	H	L	CH3
L	H	L	L	L	CH4
L	H	L	H	L	CH5
L	H	H	L	L	CH6
L	H	H	H	L	CH7
H	L	L	L	L	CH8
H	L	L	H	L	CH9
H	L	H	L	L	CH10
H	L	H	H	L	CH11
H	H	L	L	L	CH12
H	H	L	H	L	CH13
H	H	H	L	L	CH14
H	H	H	H	L	CH15

1/ Between CH0-15 and OUTPUT1 (0-15)

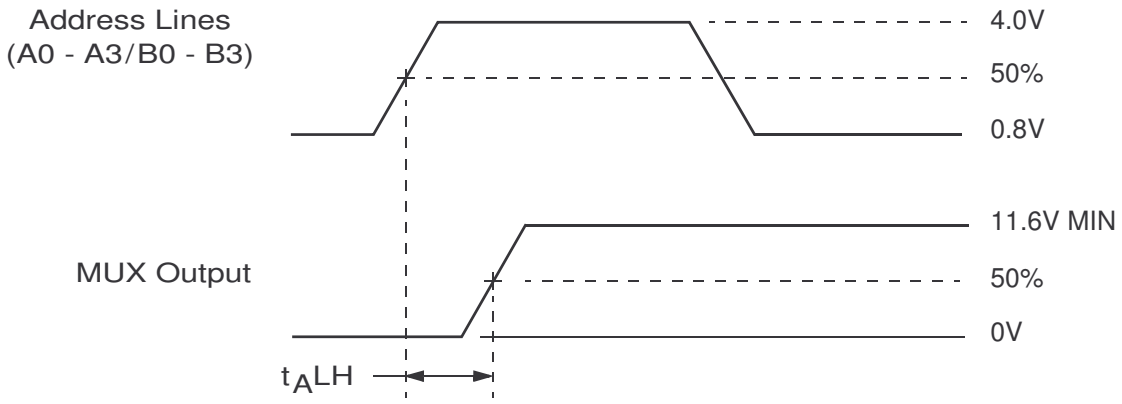
TRUTH TABLE (CH16 – CH31)

B3	B2	B1	B0	$\overline{EN}$ (16-31)	"ON" CHANNEL, 1/ (OUTPUT 2)
X	X	X	X	H	NONE
L	L	L	L	L	CH16
L	L	L	H	L	CH17
L	L	H	L	L	CH18
L	L	H	H	L	CH19
L	H	L	L	L	CH20
L	H	L	H	L	CH21
L	H	H	L	L	CH22
L	H	H	H	L	CH23
H	L	L	L	L	CH24
H	L	L	H	L	CH25
H	L	H	L	L	CH26
H	L	H	H	L	CH27
H	H	L	L	L	CH28
H	H	L	H	L	CH29
H	H	H	L	L	CH30
H	H	H	H	L	CH31

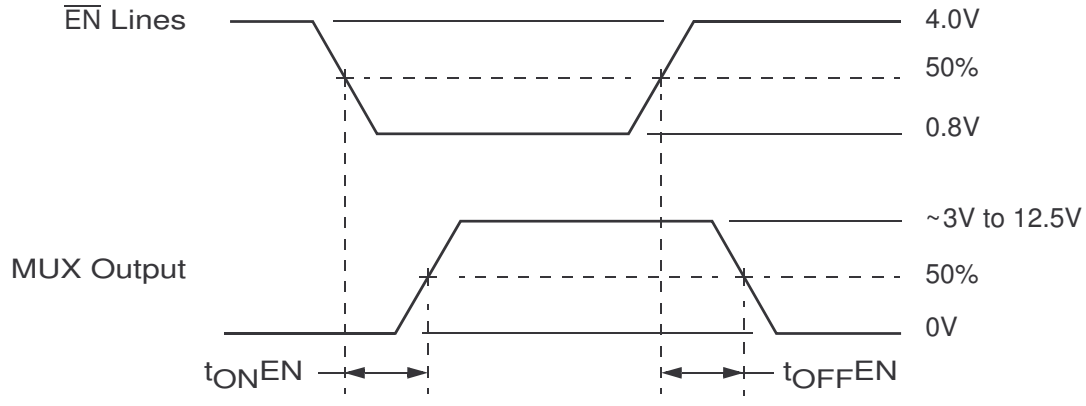
1/ Between CH16-31 and OUTPUT2 (16-31)



Definition of t_AHL



Definition of t_ALH



Definition of $t_{ON}EN$ and $t_{OFF}EN$

NOTE: f = 10KHz, Duty cycle = 50%.

MUX8533 SWITCHING DIAGRAMS

PIN NUMBERS & FUNCTIONS

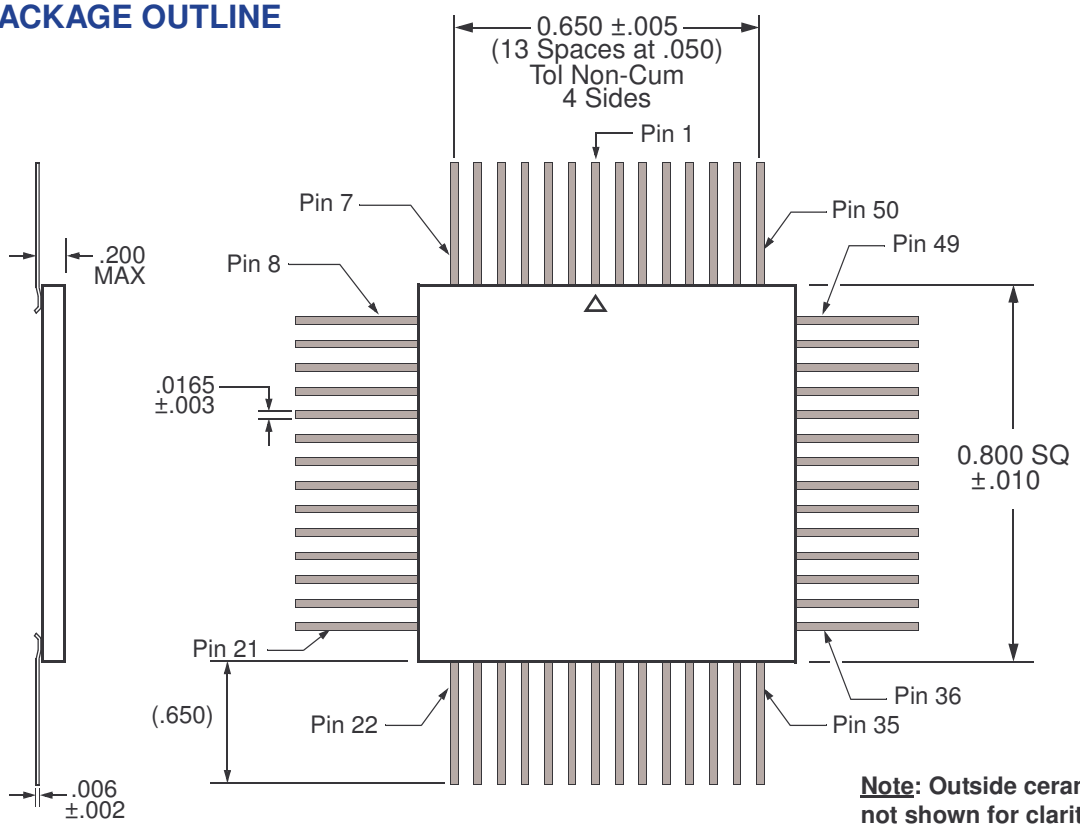
MUX8533 – 56 Leads Ceramic QUAD Flat Pack			
Pin #	**Function**	**Pin #**	**Function**
1	CH0	29	CH31
2	CH1	30	CH30
3	CH2	31	CH29
4	CH3	32	CH28
5	CH4	33	CH27
6	CH5	34	CH26
7	GND	35	GND
8	GND	36	GND
9	CH6	37	CH25
10	CH7	38	CH24
11	CASE GND	39	V_{REF}
12	OUTPUT1 (0-15)	40	B3
13	$\overline{EN}$ 0-15	41	B2
14	A0	42	B1
15	A1	43	B0
16	A2	44	$\overline{EN}$ 16-31
17	A3	45	OUTPUT2 (16-31)
18	$+V_{EE}$	46	$-V_{EE}$
19	CH15	47	CH16
20	CH14	48	CH17
21	GND	49	GND
22	GND	50	GND
23	CH13	51	CH18
24	CH12	52	CH19
25	CH11	53	CH20
26	CH10	54	CH21
27	CH9	55	CH22
28	CH8	56	CH23

Notes:
1. It is recommended that all "NC" or "no connect pin", be grounded. This eliminates or minimizes any ESD or static buildup.
2. Package lid is internally connected to circuit ground (Pins 7, 8, 11, 21, 22, 35, 36, 49, 50).

ORDERING INFORMATION

Model	DSCC SMD #	Screening	Package
MUX8533-S	-	Military Temperature, -55°C to +125°C Screened in accordance with MIL-PRF-38534, Class K	QUAD Flat Pack
MUX8533-7	-	Commercial Flow, +25°C testing only	
MUX8533-201-1S	5962-0923202KXC (Pending)	In accordance with DSCC SMD	

PACKAGE OUTLINE



Note: Outside ceramic tie bars not shown for clarity. Contact factory for details.

EXPORT CONTROL:

This product is controlled for export under the International Traffic in Arms Regulations (ITAR). A license from the U.S. Department of State is required prior to the export of this product from the United States.

EXPORT WARNING:

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A Radiation Hardened High Voltage 16:1 Analog Multiplexer for Space Applications (NGCP3580)

[Published in 2008 NSREC Radiation Effects Data Workshop Proceedings, pp 82-84]

Dennis A. Adams, Herbert A. Barnes, Michael D. Fitzpatrick, Norman P. Goldstein, William L. Hand, William L. Jackson, Rocky Koga, Michael B. Pennock, Henry J. Remenapp, Joseph T. Smith

***Abstract* – Many space systems require the multiplexing of high voltage analog signals around the spacecraft to drive actuators and motors for telemetry control. While considerable resources have supported the radiation hardening of digital electronics, very little has been focused on this critical high voltage analog requirement. To address this issue, Northrop Grumman has developed a radiation hardened high voltage (+/-15 V) 16:1 analog multiplexer for space applications which is described. This device has completed qualification testing with initial production deliveries beginning in January, 2008. Using a combination of process (CMOS/ SOI) and design techniques, this device features latch-up immune operation and 300 krad(Si) total dose hardness. Life testing has been successfully completed (1000 hours at +150 C). The NGCP3580 has been designed to operate with Analog Inputs as high as 10 V outside of the +/-15 V supply voltage range. A low voltage (+/-5 V) version of this device (NGCL3571) has been in production since 2001.**

I. Key Features for NGCP3580

- 30 V CMOS using SOI starting material
- Total Dose up to 300 krad (Si)
- Up to 40 V maximum operating voltage (Nominal: +/-15 V)

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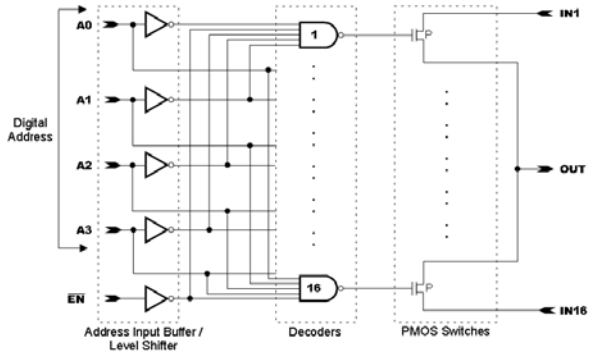


Fig. 1. NGCP3580 HV 16:1 Analog MUX block diagram

- < 500 Ohm nominal PMOS ON switch impedance
- < 1500 Ohm worst case PMOS ON switch impedance
- Break-before-make switching
- < 500 ns access time over temperature and post rad
- > 100 MOhm OFF switch impedance
- High OFF state impedance maintained under powered down conditions - ideal for redundant applications
- Low power dissipation: <500 **uA** standby current
- >1 kV electrostatic discharge protection (human body)
- Available in 28 pin ceramic flatpacks, or bare die
- SEL / SEU immune (by design)

II. HV 16:1 Analog Multiplexer Functional Description

The NGCP3580 has 16 Analog Inputs that are selected one at a time by the state of four Address Pins and an Enable- Bar pin (Fig. 1). Address and EnableBar inputs use 5V CMOS logic levels that are internally level shifted to +/-15 V to drive the high voltage Analog Input switches.

The EnableBar input serves as a Chip Select pin for use in redundant applications. Internal delays have been implemented in the design to give a nominal break-before-make delay of 50 nsec (25 nsec over temperature). This

feature prevents inadvertent damage at system level from multiple Analog Inputs being turned on at the same time. Functional operation is maintained with high OFF state impedances for over-voltage stress conditions on the 16 Analog Input and Output pins as well as on the V+ supply pin. Any of these pins may be taken up as high as +25 V. (While this is not a recommended long term operating condition for this device, devices have successfully passed 1 week burn in at +150 C with this over-voltage stress with no adverse effects noted.) Since the Analog Input switches are PMOS transistors, Analog Input ON resistance values are only guaranteed for an Analog Input range of -5 V to +25 V. (Below -5 V, the gate voltage applied to the PMOS switches is insufficient to give acceptable switch ON resistance). High Analog Input switch OFF impedance (>100 MOhm) is maintained for Analog Input levels between -25 V and +25V (with a maximum voltage difference of 40 V between the Analog Inputs / OUT pins and the supply voltage pins).

III. Process Description

The HV Analog Multiplexer process utilizes low voltage (LV = 15 V) and high voltage (HV = 40 V) CMOS transistors. All CMOS transistors have a maximum gate electric field of < 4 MV/cm under worst case allowable over-voltage stress conditions. Minimum CMOS drain breakdown is 28 V for LV CMOS and 55 V for HV CMOS. Bonded SOI wafer substrates are used which provide improved transistor to transistor isolation. All PMOS and NMOS transistors have been placed in separate N type tubs which eliminates the possibility of latch-up in this device (as confirmed with heavy ion testing). A high reliability interconnect system is used (Titanium / Aluminum / Titanium-tungsten). This same interconnect system is employed in all NGC EEPROM products that have over 15 years of reliable flight heritage. In addition, long term life testing has been performed for over 300,000 device-hours on the EEPROM product with no failures.

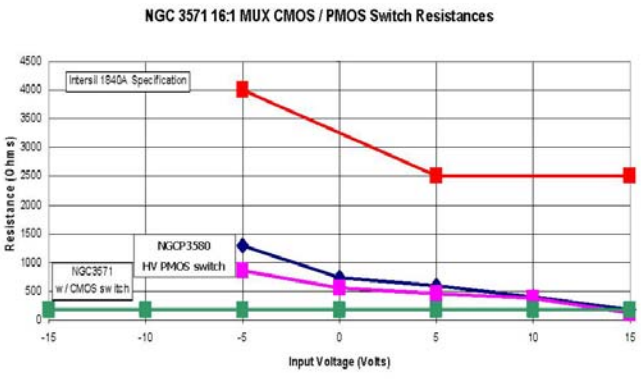


Fig. 2. NGCP3580 offers 2X improvement in Analog Input ON resistance over Intersil 1840A HV MUX.

IV. Electrical Parameters

The NGCP3580 has low power dissipation across the military temperature range for space applications - <500 uA power supply standby current, < 500 nA Analog Input leakage and < 5 uA Output leakage. Worst case Analog Input switch resistance is 1500 Ohms for Inputs at 0 or +5 V and 800 Ohms for Inputs at +15 V. This represents a resistance improvement greater than a factor of 2 over other commercially available devices (Fig. 2). Worst case access time is 500 nsec.

V. Radiation Hardness

Total dose (Cobalt 60) and heavy ion (Berkeley cyclotron) radiation testing has successfully been completed. Total dose testing was performed at the University of Maryland Cobalt 60 facility out to 450 krad(Si) (with a 1 week at +100 C rebound anneal) in accordance with MIL-STD-883-Method 1019. All parts remained spec compliant with negligible change at 300 krad, 450 krad and after rebound anneal (Figs. 3, 4). Data in the rest of these figures are shown in box plot format. The boxes represent the middle 50% of the data, with a line in the middle of the box to show the median value for the population. The whiskers on the boxes extend to the extreme value for the data or to no more than 1.5 times the box height. Any values beyond this are considered outliers. Box plots provide an excellent comparison of groups of data comparing both central values and the degree of scatter.

Heavy ion testing was performed by the Aerospace Corporation on the Berkeley cyclotron at +125 C to a maximum LET of 90 MeV-cm**2/mg with no latch-up induced (3 parts, 2E7 ions /cm**2, 30% overvoltage). A combinatorial logic design approach is used for this part (ie – no data latches). This makes this part immune to any single event upset (SEU) related failures. (Single event transients propagate through the part without being latched.)

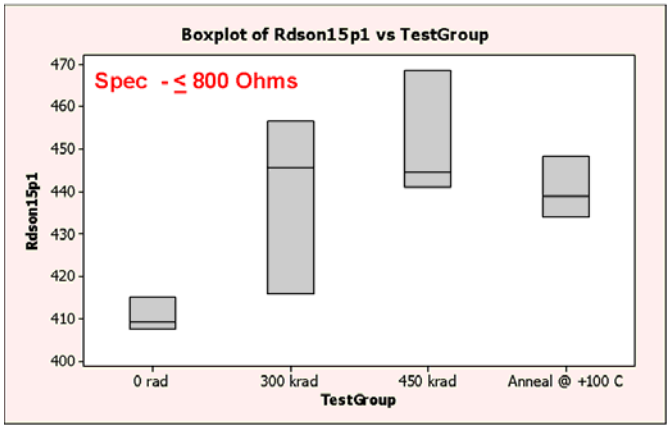


Fig. 3. Minimal change in Analog Input switch resistance with 450 krad(Si) total ionizing dose and rebound anneal.

VI. Product Qualification (Hi Rel / ClassK)

The NGCP3580 has successfully passed an extended 1000 hour life test in accordance with MIL-STD-883G Method 1005. This test was performed at elevated temperature (+150 C vs +125 C requirement) and for an additional 500 hours. A sample of 45 parts showed no loss of functionality and negligible changes in all parameters with this life test. Figs. 5, 6 and 7 show typical parametric results from this testing. All production lots are subjected to destructive SEM analysis according to MIL-STD-883 Method 2018 as well as environmental tests, dynamic burn in and total ionizing dose testing.

VII. Summary

A radiation hardened CMOS / SOI high voltage 16:1 Analog Multiplexer device has successfully completed modified hi-rel qualification and is in production. Latch-up immune operation and >300 krad total dose hardness has been demonstrated. With the recent successful completion of Class K element evaluation, the NGCP3580 high-voltage analog 16:1 MUX is now available in both die and packaged configurations for the most demanding flight applications. This device provides a high performance, cost effective solution for many critical space payload applications where the multiplexing of high voltage analog signals is required.

VIII. Acknowledgments

We would like to acknowledge the independent funding support provided by Northrop Grumman Corporation for this project.

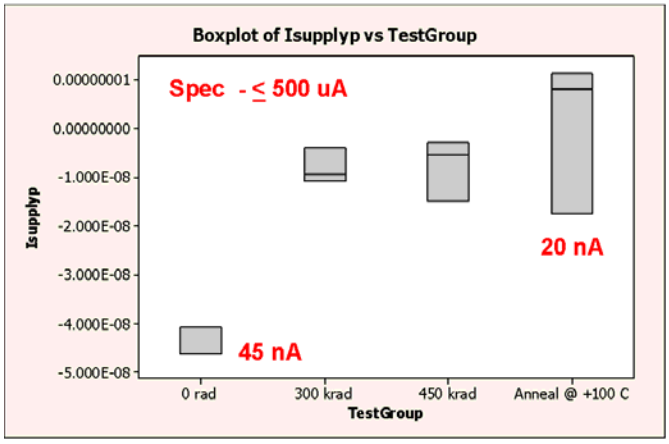


Fig. 4. Negligible change in standby supply current with 450 krad(Si) total ionizing dose and rebound anneal.

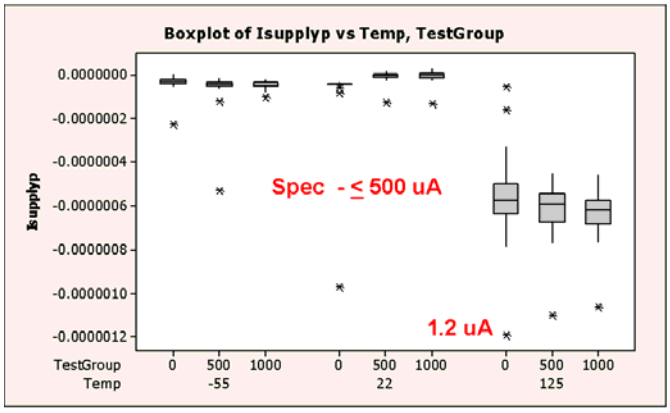


Fig. 5. Negligible change in NGCP3580 supply currents across military temperature range after 500 hours and 1000 hours at +150C (45 parts).

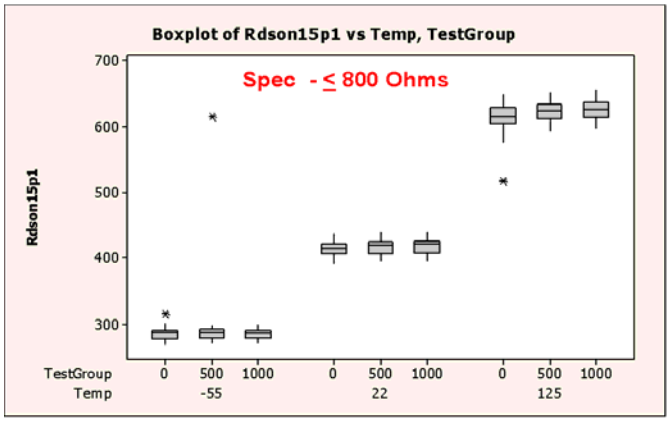


Fig. 6. Negligible change in NGCP3580 ON resistances across military temperature range after 500 hours and 1000 hours at +150C (45 parts).

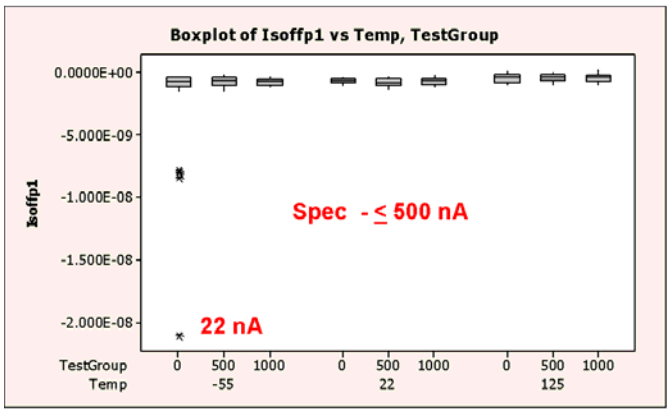


Fig. 7. Negligible change in NGCP3580 switch leakage currents across military temperature range after 500 hours and 1000 hours +150C (45 parts).

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

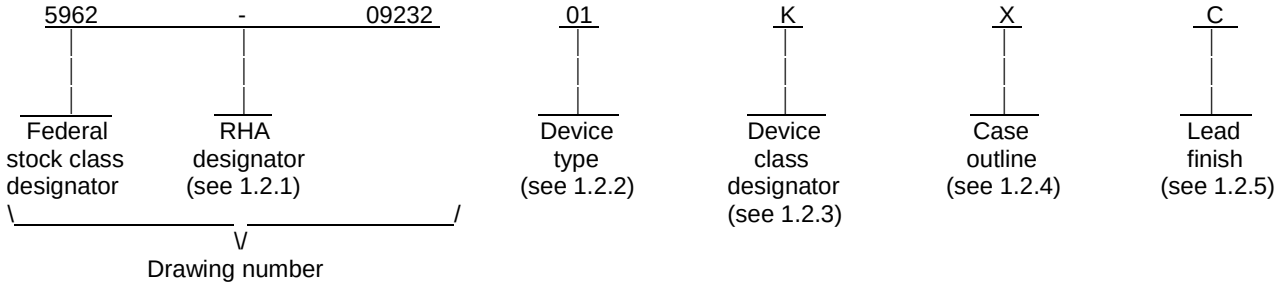
REV																				
SHEET																				
REV																				
SHEET	15	16	17																	
REV STATUS				REV																
OF SHEETS				SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A	PREPARED BY Steve Duncan	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43218-3990** http://www.dscc.dla.mil/
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Greg Cecil	
	APPROVED BY Charles F. Saffle	**MICROCIRCUIT, HYBRID, LINEAR, DUAL 16 CHANNEL, ANALOG MULTIPLEXER**
	DRAWING APPROVAL DATE **10-02-03**	
	REVISION LEVEL	SIZE: A; CAGE CODE: **67268**; **5962-09232**
		SHEET 1 OF 17

1. SCOPE

1.1 Scope. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	MUX8532	Dual 16 channel analog multiplexer, high impedance analog input
02	MUX8533	Dual 16 channel analog multiplexer, high impedance analog input with ESD protection

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

Device class	Device performance documentation
K	Highest reliability class available. This level is intended for use in space applications.
H	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C, and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	56	Ceramic quad flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Positive supply voltage between $+V_{EE}$ and GND	+20 V dc
Negative supply voltage between $-V_{EE}$ and GND	-20 V dc
V_{REF} to GND	+7.5 V dc
Digital input overvoltage range:	
V_{EN} (pins 13 and 44)	($< V_{REF}$ + .5)V, (> GND - .5)V
V_A (pins 14, 15, 16, and 17)	($< V_{REF}$ + .5)V, (> GND - .5)V
V_B (Pins 40,41,42, and 43)	($< V_{REF}$ + .5)V, (> GND - .5)V
Analog input overvoltage range:	
Device type 01	-30 V dc $\leq V_{IN} \leq$ +30 V dc
Device type 02	-18 V dc $\leq V_{IN} \leq$ +18 V dc
Power dissipation (P_D), T_C = -55°C to +125°C	40 mW
Thermal resistance junction-to-case (θ_{JC})	10°C/W 2/
Storage temperature	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Positive supply voltage ($+V_{EE}$) 3/	+15 V dc
Negative supply voltage ($-V_{EE}$) 3/	-15 V dc
V_{REF} 3/	+5 V dc
Logic low level voltage (V_{AL})	+0.8 V dc
Logic high level voltage (V_{AH})	+4.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

1/ Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Based on the maximum power dissipation spread over the multiplexer die.
3/ Supply voltages must be applied simultaneously or with the $-V_{EE}$ and V_{REF} supplies first followed by the $+V_{EE}$ supply.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 shall include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify or optimize the tests and inspections herein, however the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Switching waveform(s). The switching waveform(s) shall be as specified on figure 4.

3.2.5 Block diagram. The block diagram shall be as specified on figure 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Supply currents	$+I_{EE}$	$V_{EN(0-15)} = V_{EN(16-31)} = V_{A(0-3)} = V_{B(0-3)} = 0$	1,2,3	All	0	1	mA
	$-I_{EE}$	$V_{EN(0-15)} = V_{EN(16-31)} = V_{A(0-3)} = V_{B(0-3)} = 0$	1,2,3	All	-1	0	mA
	$+I_{SBY}$	$V_{EN(0-15)} = V_{EN(16-31)} = 4$ V, $V_{A(0-3)} = V_{B(0-3)} = 0$ 3/	1,2,3	All	0	1	mA
	$-I_{SBY}$	$V_{EN(0-15)} = V_{EN(16-31)} = 4$ V, $V_{A(0-3)} = V_{B(0-3)} = 0$ 3/	1,2,3	All	-1	0	mA
Address input currents	$I_{AL(0-3)A}$	$V_A = 0$ V	1,2,3	All	-1	1	µA
	$I_{AH(0-3)A}$	$V_A = 5$ V	1,2,3	All	-1	1	µA
	$I_{AL(0-3)B}$	$V_B = 0$ V	1,2,3	All	-1	1	µA
	$I_{AH(0-3)B}$	$V_B = 5$ V	1,2,3	All	-1	1	µA
Enable input current	$I_{ENL(0-15)}$	$V_{EN(0-15)} = 0$ V	1,2,3	All	-1	1	µA
	$I_{ENH(0-15)}$	$V_{EN(0-15)} = 5$ V	1,2,3	All	-1	1	µA
	$I_{ENL(16-31)}$	$V_{EN(16-31)} = 0$ V	1,2,3	All	-1	1	µA
	$I_{ENH(16-31)}$	$V_{EN(16-31)} = 5$ V	1,2,3	All	-1	1	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Positive input leakage current (CH0-CH31)	$+I_{SOFFOUTPUT(ALL)}$	V_{IN} = +10 V, V_{EN} = 4 V, output and all unused inputs = -10 V 4/ 5/	1,2,3	01	-200	+200	nA
				02	-100	+1000	
Negative input leakage current (CH0-CH31)	$-I_{SOFFOUTPUT(ALL)}$	V_{IN} = -10 V, V_{EN} = 4 V, output and all unused inputs = +10 V 4/ 5/	1,2,3	01	-200	+200	nA
				02	-100	+1000	
Positive output leakage current outputs (pins 12 and 45)	$+I_{DOFFOUTPUT(ALL)}$	V_{OUT} = +10 V, V_{EN} = 4 V, output and all unused inputs = -10 V 5/ 6/	1,2,3	All	-100	+100	nA
Negative output leakage current outputs (pins 12 and 45)	$-I_{DOFFOUTPUT(ALL)}$	V_{OUT} = -10 V, V_{EN} = 4 V, output and all unused inputs = +10 V 5/ 6/	1,2,3	All	-100	+100	nA
Input clamped voltage (CH0-CH31)	+VCLMP	VEN = 4 V, all unused inputs are open 5/	1	02	18.0	23.0	V
			2		18.0	23.5	
			3		17.5	22.5	
	-VCLMP	VEN = 4 V, all unused inputs are open 5/	1	02	-23.0	-18.0	V
			2		-23.5	-18.0	
			3		-22.5	-17.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Switch ON resistance outputs (pins 12 and 45) 8/	$R_{DS(ON)(0-31)A}$	V_{IN} = +15 V, V_{EN} = 0.8 V, I_{OUT} = -1 mA 4/ 5/ 7/	1,2,3	All	200	1000	Ω
	$R_{DS(ON)(0-31)B}$	V_{IN} = +5 V, V_{EN} = 0.8 V, I_{OUT} = -1 mA 4/ 5/ 7/	1,2,3	All	200	1500	Ω
	$R_{DS(ON)(0-31)C}$	V_{IN} = -5 V, V_{EN} = 0.8 V, I_{OUT} = +1 mA 4/ 5/ 7/	1,2,3	All	200	2500	Ω
Switching tests	t_AHL	R_L = 10 kΩ, C_L = 50 pF, See figure 4	9,10,11	All	10	1000	ns
	t_ALH	R_L = 10 kΩ, C_L = 50 pF, See figure 4	9,10,11	All	10	1000	ns
	$t_{ON}EN$	R_L = 1 kΩ, C_L = 50 pF, See figure 4	9,10,11	All	10	1000	ns
	$t_{OFF}EN$	R_L = 1 kΩ, C_L = 50 pF, See figure 4	9,10,11	All	10	1000	ns

1/ $+V_{EE}$ = +15 V dc, $-V_{EE}$ = -15 V dc, and V_{REF} = +5 V dc, unless otherwise specified.

2/ Measure inputs sequentially. Ground all unused inputs.

3/ If not tested, shall be guaranteed to the limits specified in table I.

4/ V_{IN} is the applied input voltage to the input channels (CH0-CH31).

5/ V_{EN} is the applied input voltage to the enable lines $\overline{EN}$(0-15) and $\overline{EN}$(16-31).

6/ V_{OUT} is the applied input voltage to the output lines OUTPUT1(0-15) and OUTPUT2 (16-31).

7/ Negative current is the current flowing out of each of the pins. Positive current is the current flowing into each of the pins.

8/ The device types 01 and 02 cannot be operated with analog inputs from -15 V to -5 V.

Case outline X.

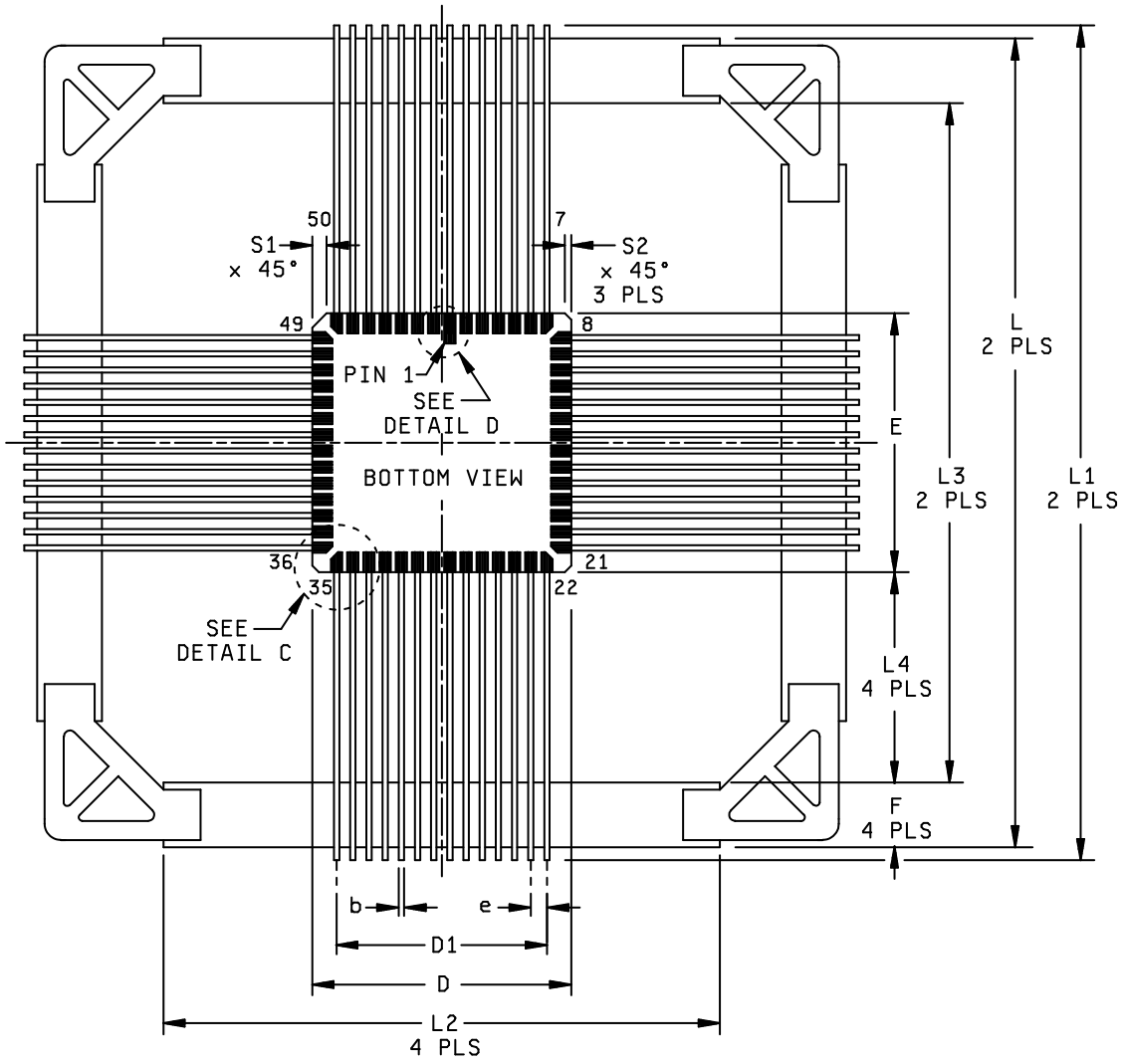


FIGURE 1. Case outline(s).

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-09232
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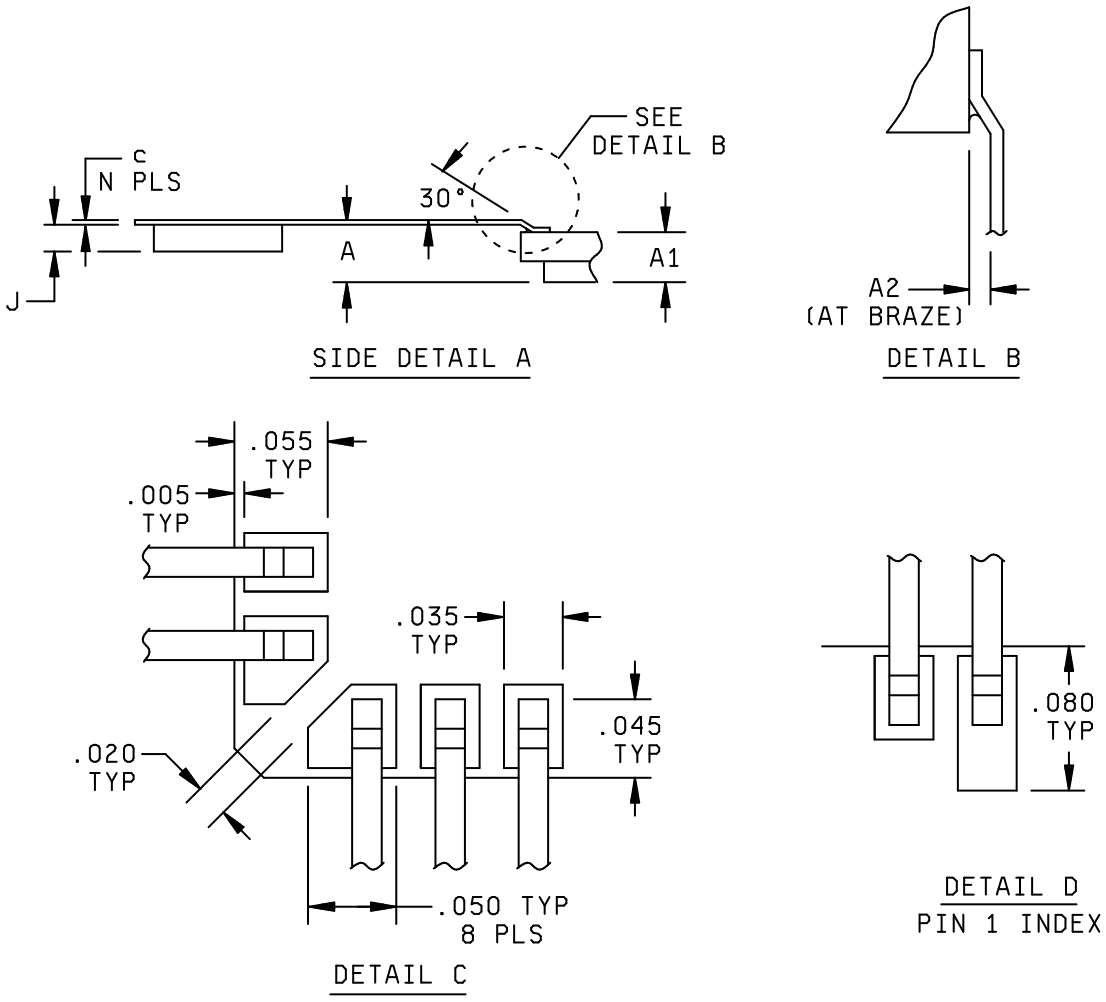


FIGURE 1. Case outline(s) - Continued.

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		.190		4.83
A1	.139	.170	3.53	4.32
A2	.005	.011	0.13	0.28
b	.0135	.0195	0.34	0.50
c	.005	.008	0.13	0.20
D/E	.790	.810	20.07	20.57
D1	.645	.655	16.38	16.64
e	.050 BSC		1.27 BSC	
F	.200 TYP		5.08 TYP	
J	.035 TYP		0.89 TYP	
L	2.490	2.510	63.25	63.75
L1		2.580		65.53
L2	1.700	1.740	43.18	44.20
L3	2.090	2.110	53.09	53.59
L4	.650 TYP		16.51 TYP	
N	56		56	
S1	.030 TYP		0.76 TYP	
S2	.015 TYP		0.38 TYP	

NOTES:
1. Pin 1 is indicated by an ESD triangle on top of the package and by an index on the bottom of the package.
2. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
3. N equals 56, the total number of leads on the package.
4. Pin numbers are for reference only.

FIGURE 1. Case outline(s) - Continued.

Device types	01 and 02		
Case outline	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	CH0	29	CH31
2	CH1	30	CH30
3	CH2	31	CH29
4	CH3	32	CH28
5	CH4	33	CH27
6	CH5	34	CH26
7	GND	35	GND
8	GND	36	GND
9	CH6	37	CH25
10	CH7	38	CH24
11	CASE GND	39	V_{REF}
12	OUTPUT1 (0-15)	40	B3
13	$\overline{EN}$ (0 – 15)	41	B2
14	A0	42	B1
15	A1	43	B0
16	A2	44	$\overline{EN}$ (16 – 31)
17	A3	45	OUTPUT2 (16-31)
18	$+V_{EE}$	46	$-V_{EE}$
19	CH15	47	CH16
20	CH14	48	CH17
21	GND	49	GND
22	GND	50	GND
23	CH13	51	CH18
24	CH12	52	CH19
25	CH11	53	CH20
26	CH10	54	CH21
27	CH9	55	CH22
28	CH8	56	CH23

NOTE:

1. Package lid is internally connected to circuit ground (Pins 7, 8, 11, 21, 22, 35, 36, 49, and 50).

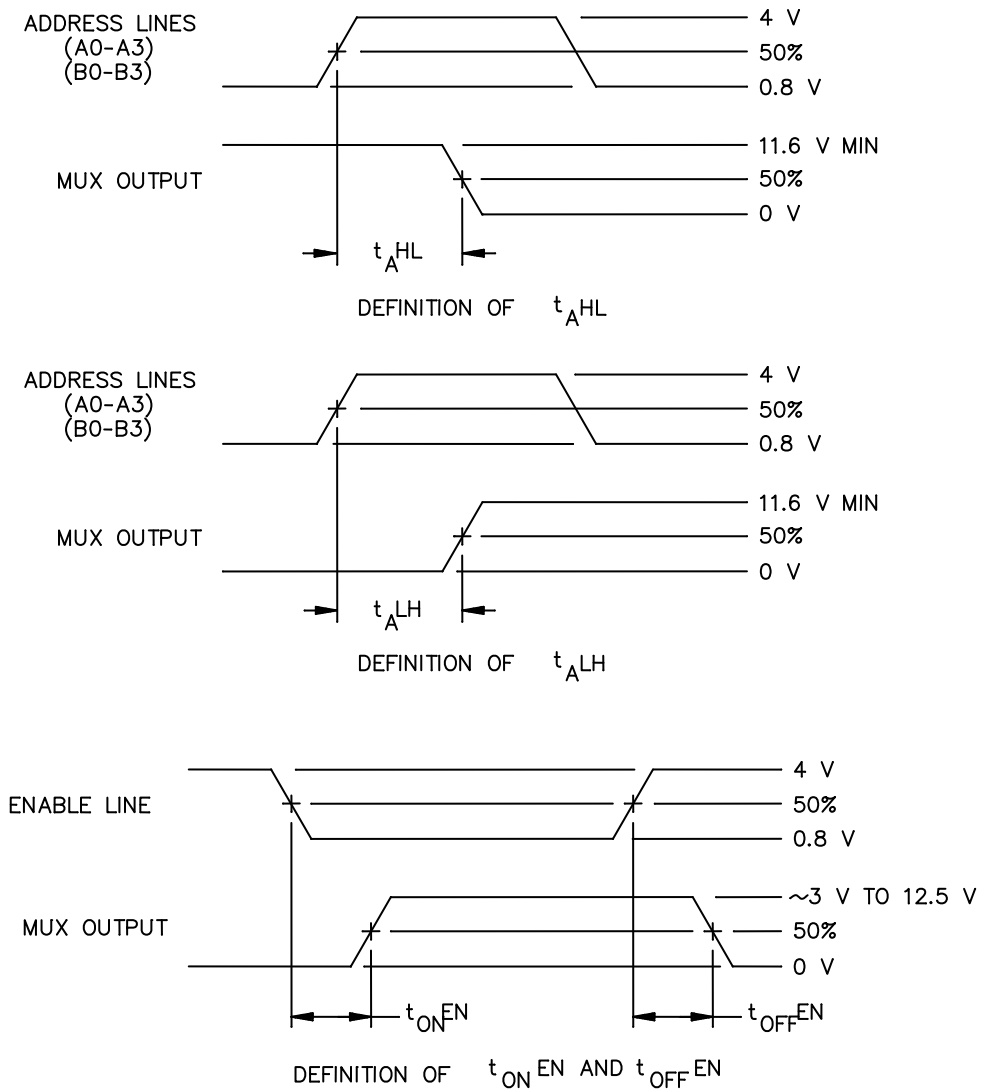
FIGURE 2. Terminal connections.

Truth table (CH0 - CH15)					
A3	A2	A1	A0	$\overline{EN}$ (0-15)	"ON" Channel OUTPUT1 1/
X	X	X	X	H	None
L	L	L	L	L	CH0
L	L	L	H	L	CH1
L	L	H	L	L	CH2
L	L	H	H	L	CH3
L	H	L	L	L	CH4
L	H	L	H	L	CH5
L	H	H	L	L	CH6
L	H	H	H	L	CH7
H	L	L	L	L	CH8
H	L	L	H	L	CH9
H	L	H	L	L	CH10
H	L	H	H	L	CH11
H	H	L	L	L	CH12
H	H	L	H	L	CH13
H	H	H	L	L	CH14
H	H	H	H	L	CH15

Truth table (CH16 - CH31)					
B3	B2	B1	B0	$\overline{EN}$ (16-31)	"ON" Channel OUTPUT2 2/
X	X	X	X	H	None
L	L	L	L	L	CH16
L	L	L	H	L	CH17
L	L	H	L	L	CH18
L	L	H	H	L	CH19
L	H	L	L	L	CH20
L	H	L	H	L	CH21
L	H	H	L	L	CH22
L	H	H	H	L	CH23
H	L	L	L	L	CH24
H	L	L	H	L	CH25
H	L	H	L	L	CH26
H	L	H	H	L	CH27
H	H	L	L	L	CH28
H	H	L	H	L	CH29
H	H	H	L	L	CH30
H	H	H	H	L	CH31

1/ Between (CH0 - CH15) and OUTPUT1 (0 - 15).
2/ Between (CH16 - CH31) and OUTPUT2 (16 - 31).

FIGURE 3. Truth table.



NOTE: f = 10 kHz, duty cycle = 50%.

FIGURE 4. Switching test waveform(s).

DEVICE TYPE 01

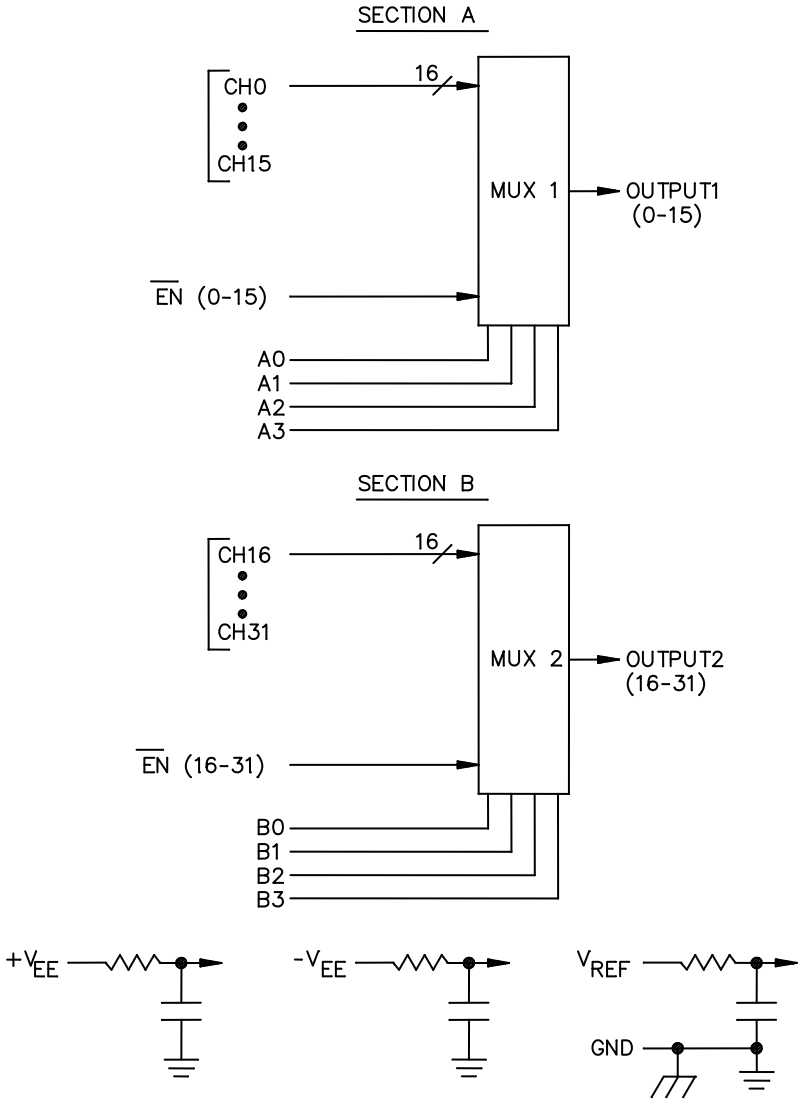


FIGURE 5. Block Diagram.

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DEVICE TYPE 02

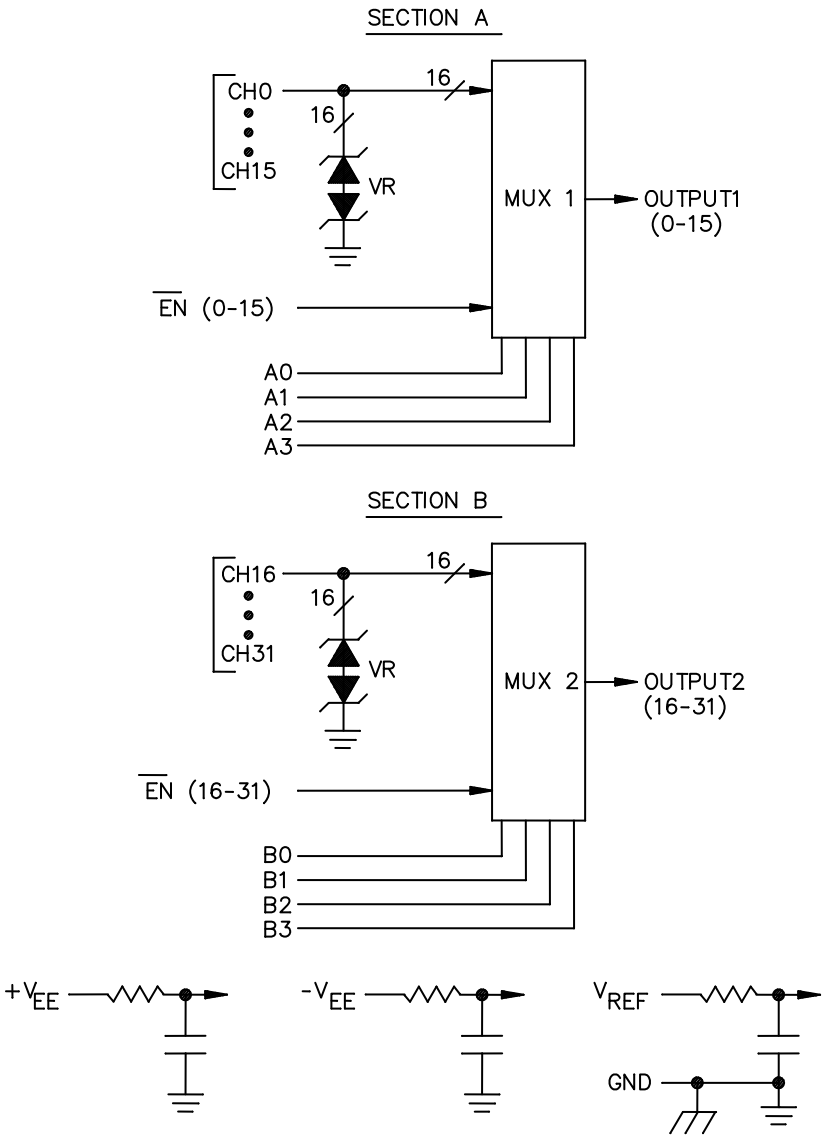

FIGURE 5. Block diagram - Continued.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1, 9
Final electrical parameters	1*, 2, 3, 9, 10, 11
Group A test requirements	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters	1, 2, 3, 9, 10, 11
End-point electrical parameters for radiation hardness assurance (RHA) devices	Not applicable

* PDA applies to subgroup 1.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 7, and 8 shall be omitted.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.

6.6 Sources of supply. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-02-03

Approved sources of supply for SMD 5962-09232 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0923201KXC	88379	MUX8532-201-1S
5962-0923202KXC	88379	MUX8533-201-1S

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
88379	Aeroflex Plainview Incorporated, (Aeroflex Microelectronics Solutions) 35 South Service Road Plainview, NY 11803-4193